PART IIB 2010 4B6 SOLID STATE DEVICES AND CHEMICAL/BIOLOGICAL SENSORS

DR D P CHU

Q1

(a) If we apply a positive (negative) voltage step to a p-type (n-type) MOS capacitor, which is sufficient to generate an inversion larger at equilibrium, there is a time interval, after the step, when no free electrons (holes) are present at the interface. This is due to the fact that the inversion charge must be thermally generated and this requires a finite time.

During such a time interval, the MOS is said to be in 'deep depletion' and the only charge present in the semiconductor is the depletion charge.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s\varepsilon_0}$$

$$\rho(x) = -qN_A$$

$$\frac{d\psi}{dx} = \frac{qN_A}{\varepsilon_s\varepsilon_0}(w-x)$$

$$\psi_S = \frac{qN_A}{2\varepsilon_s\varepsilon_0}w^2$$

$$w = \left(\frac{2\varepsilon_s\varepsilon_0}{qN_A}\psi_S\right)^{\frac{1}{2}}$$

$$Q_S = Q_B = qN_A w$$

which proves the required equation. [30%]

(b) $V_G = V_i + \psi_s$

$$V_i = \frac{Q_B}{\epsilon_i} d$$

$$Q_B = -\left[2\,\epsilon_s\, q\, N_A\, \psi_s\right]^{1/2}$$

$$V_G = \frac{\left[2\epsilon_s\, q\, N_A\, \psi_s\right]^{1/2} d}{\epsilon_i} + \psi_s = 5.06\text{V}$$

[20%]

(c) $w = \left(\frac{2\varepsilon_s\varepsilon_0}{qN_A}\psi_S\right)^{\frac{1}{2}} = 2.29 \times 10^{-6}$ m [10%]

(d)

$$1/C_{tot} = 1/C_D + 1/C_i = \frac{w}{\varepsilon_s\varepsilon_0} + \frac{d}{\varepsilon_{ox}}$$

$C_{tot} = 4.05 \times 10^{-5}$ Farad m^{-2} [10%]

(e) (i) In deep depletion the depletion length w increases with the pulse voltage V, so the capacitance decreases until breakdown occurs.

When the inversion charge is formed, such charge, localized very close to the insulator -semiconductor interface, screens the bulk of the semiconductor, $\psi_S \approx 2\psi_B$ and the depletion region decreases. [15%]

(ii) At low frequency the inversion charge is modulated by the ac voltage. The total semiconductor capacitance is the parallel between the inversion charge capacitance and the depletion capacitance. The latter is constant, because ψ_S and therefore w are nearly constant, while the former increases with the amount of inversion charge. Eventually the inversion charge capacitance becomes much bigger than the insulator capacitance and $C_{tot}=C_i$.

At high frequencies the inversion charge cannot follow the ac voltage and therefore the semiconductor capacitance is C_D. So $C_{tot}= C_i//C_D=$ constant. [15%]

Assessor's comment:

A popular and straightforward question, well-answered by most candidates. The only difficulty was in describing the behaviour of capacitance as a function of voltage.

Q2

(a) For a negligible V_{DS}, the threshold voltage V_T is the voltage between gate and source, V_{GS}, such that the concentration of minority carriers at the surface equals the concentration of majority carriers in the bulk.

[20%]

(b) In these conditions:

$$|E_F - E_i|surface = |E_F - E_i|bulk = q\psi_B$$

$$N_A \approx p = n_i \exp\frac{q\psi_B}{kT}$$

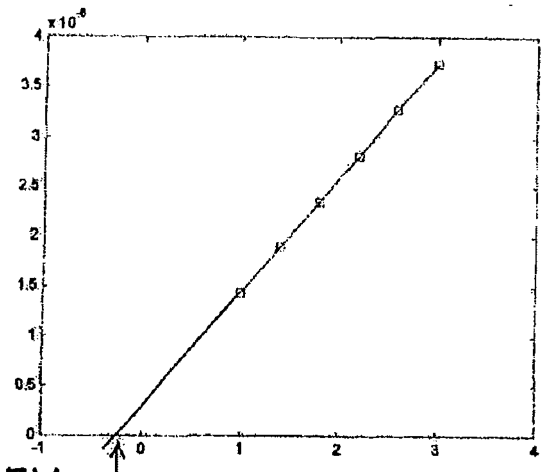
$$\psi_S = 2\psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i} = 0.618$$

$$Q_B = (2\,\varepsilon_S\, qN_A\psi_S)^{\frac{1}{2}} = -1.44x\ 10^{-8}\ C\,cm^{-2}$$

$$V_T = \psi_S + \frac{d}{\varepsilon_i}Q_B = 0.659V$$

[40%]

(c)



$V_T = -0.245V$

$$Q_F = \frac{\varepsilon_i}{d}\Delta V_T = 3.12\ x\ 10^{-3}\ C\,m^{-2}$$

[40%]

Assessor's comment

Another straightforward question. Difficult to some for the mixed types of calculations.

Q3

(a) (i) Remnant polarisation: $P_r \sim 25\ \mu C\ cm^{-2}$ [10%]

(ii) Coercive field: $E_c \sim 80\ kV\ cm^{-1}$ [10%]

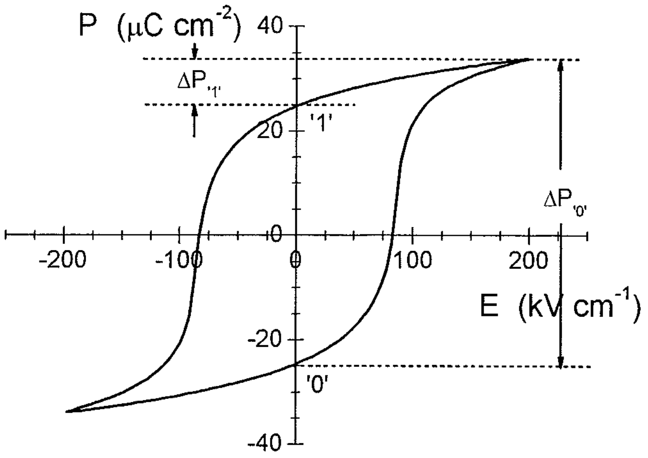
(iii) Energy density consumed in a full switching cycle:

$E \sim 2P_r{*}2E_c \sim 8\ J\ cm^{-3} = 8x10^{6}\ J\ m^{-3}$ [10%]

(b) (i) $\Delta Q = \Delta P{*}Area = (0.18\mu m{*}0.18\mu m)\ \Delta P = 3.24x10^{-10}\ cm^2\ {*}\Delta P$

$\Delta Q_{'1'} = 3.24x10^{-10}\ cm^2\ {*}\ \Delta P_{'1'} = 3.24x10^{-10}\ cm^2\ {*}(34-25)\ \mu C\ cm^{-2}$
$= 2.9x10^{-15}\ C = 2.9\ fC$

$\Delta Q_{'0'} = 3.24x10^{-10}\ cm^2\ {*}\ \Delta P_{'0'} = 3.24x10^{-10}\ cm^2\ {*}(34+25)\ \mu C\ cm^{-2}$
$= 19x10^{-15}\ C = 19\ fC$



[20%]

(ii) $V_{sense} = \Delta Q\ /\ C_{sense}$

$V_{sense,'1'} = \Delta Q_{'1'}\ /\ C_{sense} = 2.9\ fC\ /\ 2\ pF = 1.5\ mV$

$V_{sense,'0'} = \Delta Q_{'0'}\ /\ C_{sense} = 19\ fC\ /\ 2\ pF = 9.5\ mV$ [20%]

(iii) $\min(Area) = \min(V_{sense}){*}C_{sense}\ /\ \max(\Delta P) = 1mV{*}2pF/[(34+25)\mu C\ cm^{-2}]$
$= 2x10^{-15}/59x10^{-6}\ cm^2$

$= 3.38\text{x}10^{-11}\ \text{cm}^2 = 3.38\text{x}10^{-3}\ \mu\text{m}^2$
$= 58\text{nm x } 58\text{ nm}$

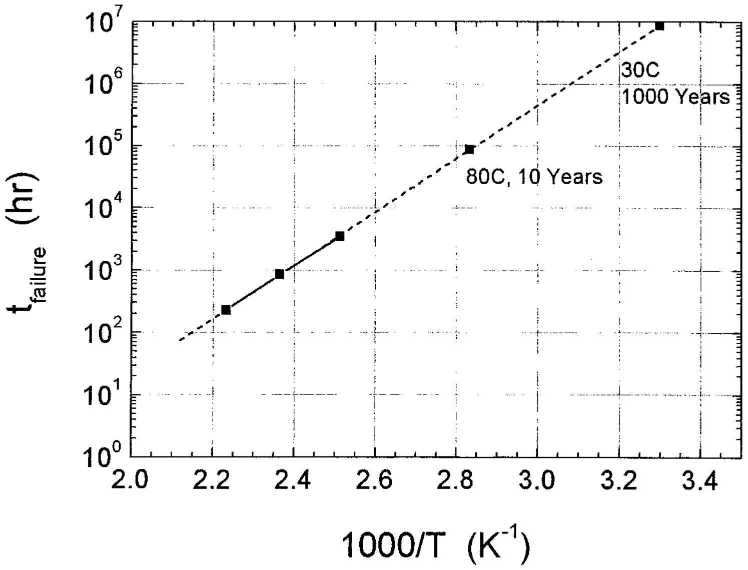
[10%]

(c) 80°C → $1000/T = 1000/(80+273) = 2.83\ (K^{-1})$

30°C → $1000/T = 1000/(30+273) = 3.30\ (K^{-1})$

$9\text{x}10^4$ hrs = $9\text{x}10^4/(24*365)$ yrs = 10.27 yrs ~ 10 yrs

$9\text{x}10^6$ hrs = $9\text{x}10^6/(24*365)$ yrs = 1027 yrs ~ 1,000 yrs



[20%]

Assessor's comment:

The most popular question, taken by all candidates. No technical problem to answer if there is a good understanding of the fundamentals.

Q4

(a) (i) A magnetic tunnel junction (MTJ) consists of two conductive magnetic layers (Co layers here) with a non-conductive non-magnetic tunnel layer (Al_2O_3 layer here) in between. The magnetisation is usually switchable only in one layer.

CPP configuration: Apply voltage across the two magnetic layers and measure the resulting current which tunnels through the non-conductive layer;

CIP configuration: Apply voltage on the same magnetic layer and measure the resulting tunnelling current. [20%]

(ii) The lower Co layer in the CIP configuration can have effect on the measured current. This is because the non-conductive tunnel layer is thin, in comparison to the electron coherence length. The spin polarisation state of the electrons flow from one electrode to the other can be altered when they are scattered of from the lower Co layer during transportation, resulting a change in scattering coefficient (depending on the magnetisation direction in the lower Co layer) when they return to the upper Co layer, hence the change in the magnitude of the measured current. Note that this is a pure quantum effect without classical correspondence. [20%]

(iii) A bit of information is physically stored in terms of the direction of magnetisations in the upper and lower Co layers. For example, the parallel (anti-parallel) configuration can be referred as State “1” (State “0”).

The magneto-resistance in a MTJ (in either the CPP or the CIP configuration) is low (high) when the magnetisation directions in the two magnetic layers are parallel (anti-parallel). Therefore, the stored bit of information can be represented by the two levels of MTJ resistance. [10%]

(b) (i) To write a bit of information is to switch the magnetisation in one of the magnetic layers (the upper one here) to the desired direction.

To avoid switching the half-selected cells, switching is performed by using a combined magnetic field induced by the electric current in the corresponding D-Line and B-Line (neither of them can do the switching on its own as shown on the right in Figure 4).

In the case of writing into B2-W2, using D2 to induce a magnetic field and switching the magnetisation half way and followed by using B2 to induce a separated magnetic field in the desired direction to complete the switching. [30%]

(ii) Select W2 to High (i.e. the transistor to ON state), apply a voltage on B2 and measure the current through it. The current level corresponds to the resistance of the MTJ at B2-W2, hence the bit of information stored in it. [10%]

(iii) A MTJ should be rectangle in shape, so that the magnetisation in the switchable layer only has two easy directions, representing the state of stored binary information. [10%]

Assessor's comment:

An unpopular question. Not so many full understand the importance of quantum effect.