

ENGINEERING TRIPOS PART IIB

Friday 30 April 2010 9 to 10.30

Module 4B6

SOLID STATE DEVICES AND CHEMICAL / BIOLOGICAL SENSORS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachment: Constants sheet (1 page)

STATIONERY REQUIREMENTS	SPECIAL REQUIREMENTS
Single-sided script paper	Engineering Data Book
Graph paper	CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. An ideal p-type silicon MOS capacitor has the following parameters:

oxide thickness	$d=10^{-7}$ m
oxide dielectric constant	$\epsilon_i=3.9\epsilon_0$
semiconductor dielectric constant	$\epsilon_s=11.9\epsilon_0$
acceptor concentration	$N_A=10^{21}$ m ⁻³

A voltage pulse of amplitude V is applied to the capacitor, resulting in a surface potential $\psi_s = 4$ V, before any appreciable inversion charge is generated (deep depletion).

- (a) Starting from Poisson's Equation:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s\epsilon_0}$$

Prove that the total charge per unit surface in the semiconductor is given by:

$$Q_B = -(2\epsilon_0\epsilon_s q N_A \psi_s)^{\frac{1}{2}} \quad [30\%]$$

- (b) Calculate V . [20%]
- (c) Calculate the length of the depletion region. [10%]
- (d) Calculate the device capacitance per unit area under these conditions. [10%]
- (e) Explain the behaviour of the capacitance as a function of V for a MOS:
- (i) In deep depletion. [15%]
- (ii) After the formation of the inversion layer, when the frequency of the AC voltage employed to measure the capacitance is low (~ 1 Hz) and when it is high (~ 100 kHz). [15%]

- 2 (a) Define the threshold voltage for a MOSFET [20%]
- (b) Calculate the threshold voltage for a silicon n-MOSFET with the following parameters:

Gate Oxide (SiO_2) thickness $d=10^{-8}$ m

Acceptor Concentration $N_A=10^{21}$ m^{-3}

Assume the device is ideal and V_{DS} is negligibly small. [40%]

- (c) N-Channel MOSFETs with the above parameters are fabricated and, due to a fault in the process, some fixed charge is present at the oxide/semiconductor interface.

From the I_D - V_{GS} data below, obtained for $V_{DS}=0.001$ V, determine the density and sign of the fixed charge.

V_{GS} (V)	I_D (10^{-6} A)
1.0	1.43
1.4	1.89
1.8	2.35
2.2	2.81
2.6	3.27
3.0	3.73

[40%]

3 (a) For the ferroelectric thin film material shown in Fig. 1, please find out the values of:

(i) remnant polarisation;

[10%]

(ii) coercive field;

[10%]

(iii) energy density consumed in a full switching cycle.

[10%]

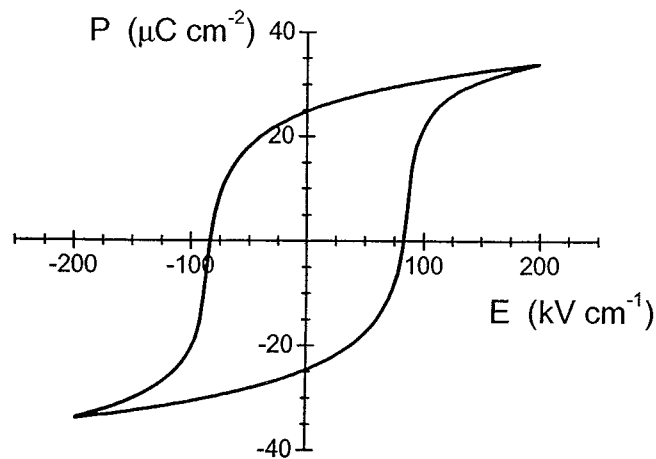


Fig. 1

(b) A ferroelectric thin film capacitor in a FRAM cell is made of the ferroelectric material shown in Fig. 1 with dimensions of 150 nm in thickness and $0.18 \mu\text{m}$ by $0.18 \mu\text{m}$ square in size.

(i) If we apply a voltage across it in the form of a positive step function with a height of +3V, what will be the switching charges if the initial information stored in this memory cell was of State '1' (positively polarised) and State '0' (negative polarised), respectively?

[20%]

- (ii) If the bit line parasitic capacitance, which is utilised as a sensing capacitor, is 2 pF, what are the sensed voltage levels for these two states, respectively?

[20%]

- (iii) Theoretically, how small can this capacitor be in order to maintain its original function as a memory cell, given that the Read-out sense amplifier has a resolution of 1 mV?

[10%]

- (c) Figure 2 shows the results of an accelerated reliability test for the above memory cell. What are the projected life times of this device at 80 °C and 30 °C, respectively? (Hint: assume $t_{\text{failure}} \sim \exp(+\Delta E/kT)$, where ΔE is a constant and k the Boltzmann constant.)

[20%]

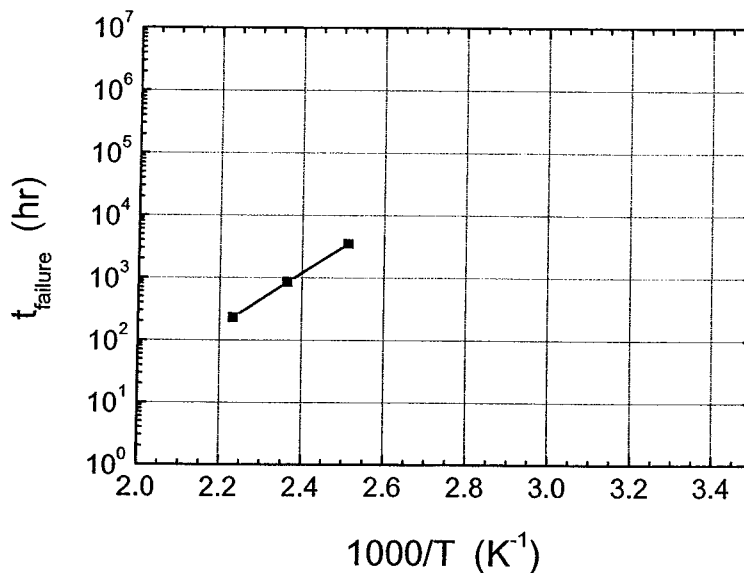


Fig. 2

4 (a) Explain:

(i) how a magnetic tunnel junction (MTJ) works in the current-perpendicular-to-plane (CPP) and current-in-plane (CIP) configurations, as shown in Fig.3, respectively;

[20%]

(ii) whether the lower Co layer, which is not in contact in the CIP configuration, has any impact on the measured current and why;

[20%]

(iii) how a bit of information is stored and which physical quantities are read-out.

[10%]

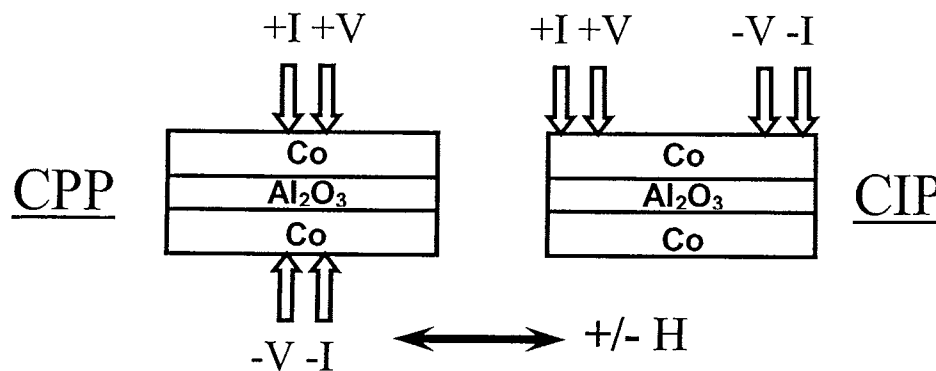


Fig.3

(b) A sketch of a MRAM array is shown on the left in Fig. 4. For a given cell (say B2-W2), explain:

(i) how to write a bit of information into the cell, with reference to the diagram on the right hand side of Fig. 4;

[30%]

(ii) how to read the stored information;

[10%]

(iii) the importance of the physical geometry of the device.

[10%]

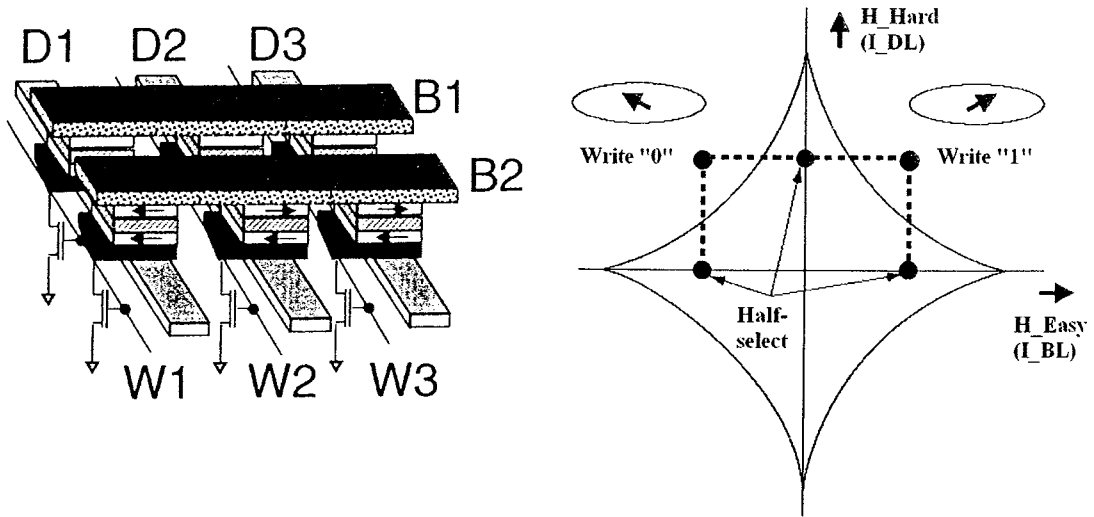


Fig. 4

END OF PAPER

Constants

** Note that not all the information below may be needed to answer the questions*

$$\epsilon_0 = 8.85 \cdot 10^{-12} \text{ Farad m}^{-1} \quad \text{permittivity in vacuum}$$

$$k = 1.38 \cdot 10^{-23} \text{ Joules K}^{-1} = 8.625 \cdot 10^{-5} \text{ eV K}^{-1} \quad \text{Boltzman constant}$$

$$kT/q = 0.025 \text{ V at } T = 300 \text{ K} \quad (\text{where } q \text{ is the absolute value of an electron charge})$$

$$N_c = 2.8 \cdot 10^{25} \text{ m}^{-3}$$

$$N_v = 1.04 \cdot 10^{25} \text{ m}^{-3}$$

$$E_g(\text{silicon}) = 1.12 \text{ eV}$$

$$\epsilon_i (\text{silicon dioxide}) = 3.9\epsilon_0$$

$$\epsilon_s (\text{silicon}) = 11.9\epsilon_0$$

$$n = N_c \exp[(E_F - E_C)/kT]$$

$$p = N_v \exp[(E_V - E_F)/kT]$$

$$(np)^{0.5} = n_i = 6.6 \cdot 10^{15} \text{ m}^{-3}$$

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Q1: (b) 5.06 V;
(c) 2.29×10^{-6} m;
(d) 4.05×10^{-5} Farad m^{-2} .

Q2: (b) 0.659 V;
(c) 3.12×10^{-3} C m^{-2} .

Q3: (a) $25 \mu\text{C cm}^{-2}$, 80 kV cm^{-1} , $8 \times 10^6 \text{ J m}^{-3}$;
(b) 2.9 fC, 19 fC; 1.5 mV, 9.5 mV; 58nm square;
(c) 10 yrs, 1,000 yrs.