ENGINEERING TRIPOS PART IIB

Monday 3 May 2010 9 to 10.30

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. A plan view showing an n-channel MOS transistor and associated interconnect structures is shown in Fig. 1. The polysilicon interconnect and gate electrode are of width 2 μm, and the metal interconnect is of width 4 μm. The interconnect lengths are as shown. The active region has dimensions 4 μm × 14 μm.

(a) Discuss briefly the origins of the key contributions to parasitic capacitances arising from the MOS device itself and the associated interconnect. [20%]

(b) Figure 2 is a table of information abstracted from the manufacturer's data about the process in use, and consists of specific capacitance values per unit area or per unit length. Using the data supplied, determine as accurately as possible the key capacitances at zero bias for this device at input and output. You may ignore the effects of contact structures for the purpose of this calculation. [40%]

(c) Indicate qualitatively how these capacitances would be expected to change if normal device operating voltages were applied. State any assumptions made. [20%]

(d) Draw a cross section through the transistor structure along the dashed line A-A', and identify the various conducting layers and their electrical function in the device. [20%]

(cont.

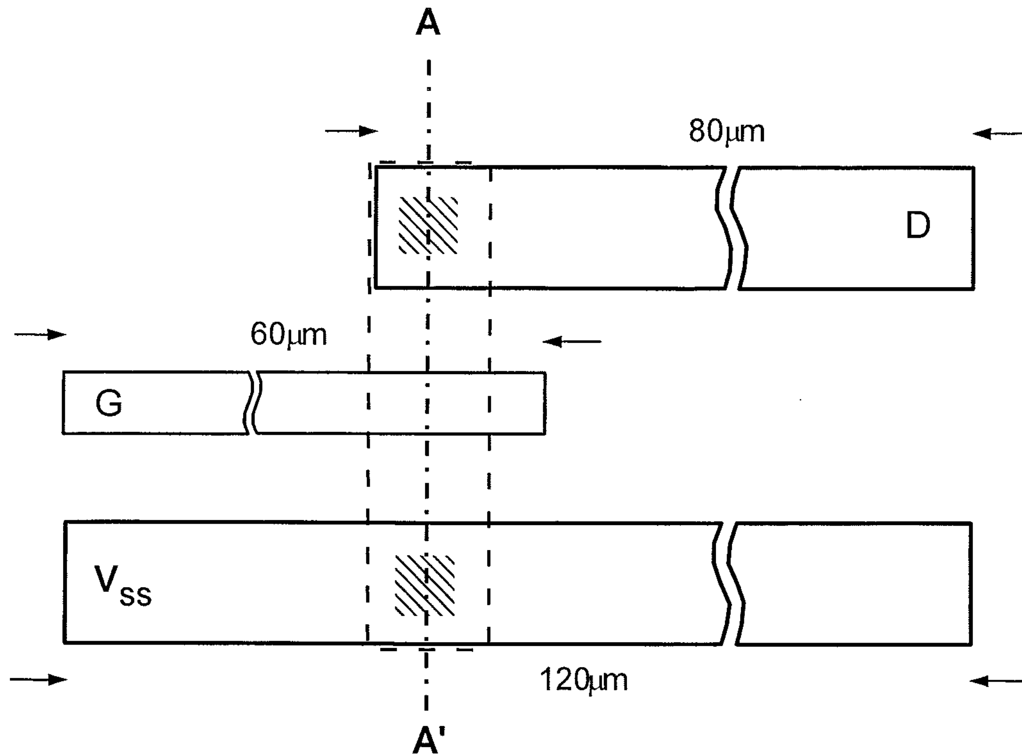

Fig. 1

Parameter	Value	Units	Description
C_O	7×10^{-4}	Fm^{-2}	Capacitance associated with gate oxide dielectric
C_{JA0}	1×10^{-4}	Fm^{-2}	Area capacitance to substrate (source or drain)
C_{JP0}	4×10^{-10}	Fm^{-1}	Peripheral capacitance to substrate (source or drain)
C_{GD0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with drain
C_{GS0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with source
C_{MA}	3×10^{-5}	Fm^{-2}	Area capacitance to substrate of metal over field oxide
C_{MP}	4×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of metal over field oxide
C_{PA}	4×10^{-5}	Fm^{-2}	Area capacitance to substrate of polysilicon over field oxide
C_{PP}	5×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of polysilicon over field oxide

Figure 2

(TURN OVER

2. (a) With a set of annotated diagrams, describe the fabrication schedule for making an NMOS transistor. [40%]

   (b) What additional steps are needed to make a CMOS transistor pair? [20%]

   (c) Comment on the refinements to CMOS technology represented by

      (i) silicon-on-insulator technology;

      (ii) multiple layer interconnects;

      (iii) hafnium oxide dielectrics; and

      (iv) Bi-CMOS. [40%]

3. (a) Why has reliability become such an important aspect of the production of integrated circuits and how is reliability achieved in practice? [30%]

   (b) Describe the bath-tub curve as a general model of failure rate analysis and comment specifically on its application to VLSI products. [30%]

   (c) Describe the failure factors, failure mechanisms, signatures of failure and the implications for a refined original design associated with each of:

      (i) the passivation of integrated circuits;

      (ii) electromigration in the metal interconnects;

      (iii) hot carrier degradation within or adjacent to the transistors; and

      (iv) electrostatic discharge. [40%]

4. The constant field model of MOS scaling applies a dimensionless factor k to manufacturing dimensions (length, width and thickness), voltages and doping densities, so that electric fields remain unchanged. For example, with $k = 1$, the dimensions are unchanged; with $k = 1.1$, they would be slightly reduced.

(a) Based on the method of dimensions, derive appropriate expressions for the consequent scaling of the following parameters:

(i) gate area;
(ii) gate delay;
(iii) parasitic capacitance;
(iv) current;
(v) static power consumption (per inverter gate);
(vi) power density (per unit area);
(vii) current density (in wires);
(viii) signal delay due to interconnect. [50%]

(b) Discuss the main implications of the effects described in (a) for size, speed and power consumption in digital CMOS designs. [20%]

(c) What further factors make this model inappropriate as device sizes continue to decrease? [30%]

5. (a) Describe the circuit structures used in CMOS technology to convey digital signals between input pads and the inputs of logic gates comprising small geometry devices. Discuss the precautions used to protect inputs from the effects of applying excessive voltages and static discharges, and to guard against latchup. [50%]

(b) Discuss quality, cost, delivery and service as critical success factors for the successful manufacture of integrated circuits. [25%]

(c) Describe some of the processes required before a manufacturing line can be approved for the production of quality-assured VLSI products. [25%]

END OF PAPER

4B7 VLSI Design, Technology and CAD - 2010 Numerical Answers

1. Cinput = 14.9 fF; Coutput = 29.1 fF

2.

3.

4.

5.