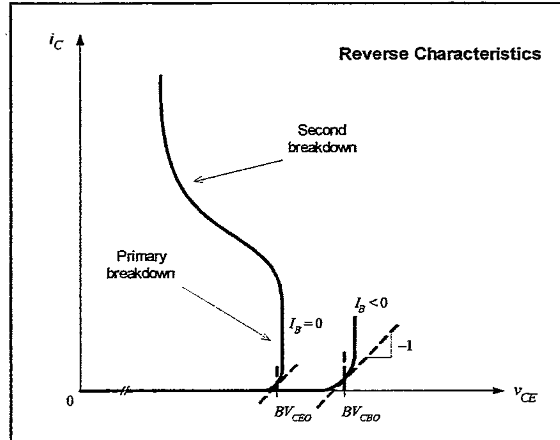
PART IIB 2011 PROF F UDREA

4B2 POWER MICROELECTRONICS SOLUTIONS

1. (a) ***Second breakdown:*** This is characterized by a snap-back in the breakdown characteristics. The *second breakdown* appears at large currents and results in a fast drop in the collector-emitter voltage. As the current increases, the temperature increases. If the temperature increases the injection is stronger and the current increases again. Hence BJTs suffer from a positive current-temperature feedback. This is known as *thermal runaway (*or the *filamentaion effect).*



[20%]

(b) $f = \frac{1}{T} = 10\text{kHz} \Rightarrow \text{T} = 100\,\mu s$, $D = 50\%$,

$DT = t_{on} + t_r + t_d = 50\mu s \Rightarrow t_{on} = 50 - 0.5 - 0.1 = 48.5\mu s$

$(1-D)T = t_{off} + t_s + t_f = 50\mu s \Rightarrow t_{off} = 50 - 5 - 3 = 42\mu s$

<u>ON -STATE</u>

$$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} \text{V}_{\text{CE}} I_{\text{C}} dt = V_{\text{CE}} I_{\text{C}} \frac{t_{on}}{T} = 2 \times 100 \times 0.485 = 97W$$

<u>TURN – ON</u>

$$P_d = \frac{1}{T}\int_0^{t_d} V_{dc} I_{OFF} dt = t_d f I_{OFF} V_{dc} = 3.75mW \text{ – (can be neglected)}$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_C \frac{t}{t_r}[V_{dc} + (V_{CE} - V_{dc})\frac{t}{t_r}]dt = t_r f I_C[\frac{V_{dc}}{2} + \frac{V_{CE} - V_{dc}}{3}] = 42.33W$$

<u>TURN – OFF</u>

Delay time: $P_s = V_{\text{CE}} I_{\text{C}} t_s f = 10W$

Current fall time:

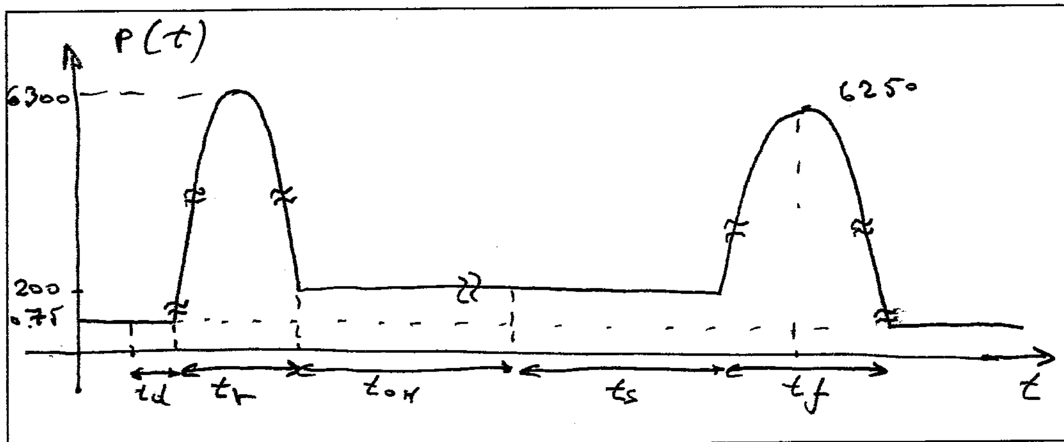
$$P_f = \frac{1}{T}\int_0^{t_f} I_C(1 - \frac{t}{t_f})V_{dc}\frac{t}{t_f} = t_f f I_C \frac{V_{dc}}{6} = 125W$$

<u>OFF -STATE</u>

$P_{OFF} = V_{\text{dc}} I_{\text{OFF}} t_{OFF} f = 0.315W$

Total losses (on-state + turn-on + turn-off):

P total= 97+42.33+ 135+ 0.315= 274.65W [40%]



[25%]

The power loss due to the base current can be calculated as:

$$P_B = V_{BE} I_B D = 4W$$ [15%]

Examiner's comment:

This was a straightforward and most popular question, well answered by virtually all candidates. Perhaps the question was too easy but it was pleasing to see that most of the candidates were able to do the power calculations for a BJT in resistive switching. Not all the candidates were able to draw a graph of the instantaneous power function of time.

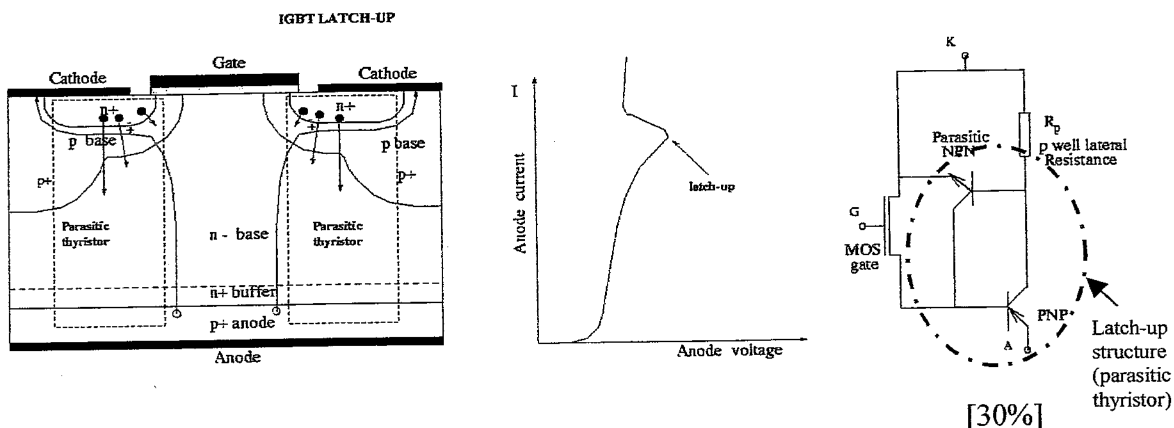
2. (a) The IGBT has a parasitic thyristor formed between the n+ cathode, p well, n- base and p+ anode. To avoid the latch-up of this thyristor, the turn-on of the upper npn transistor must be suppressed. For that the lateral resistance of the p well should be kept as small as possible to avoid the turn-on of the emitter/base junction formed between the n+ cathode and the p base. This is accomplished by :

(a) introducing a deep p+ well diffusion short-circuited to the n+ cathode diffusion through a metal layer. The effect of this is to reduce the resistance of the p well lateral diffusion which lowers the voltage drop across the emitter/base junction

(b) reducing the length of the n+ (by for example using a trench gate structure which cuts the n+ diffusion).

(c) lowering the junction temperature (as the latch-up is exarcebated at higher temperatures)

When the hole current under the n+ cathode develops a 0.7 V across the p well lateral resistance, the emitter junction of the npn transistor (i.e. cathode junction) becomes forward biased and the npn transistor turns on. This is followed by injection of electrons straight from the n+ cathode (which becomes an emitter) to the n- drift region (which acts as a collector). The npn together with the pnp will now form a thyristor feedback and the current can no longer be controlled by the gate. Moreover the IGBT in this conditions cannot be turned-off. The latch-up can also be prevented by lowering the lateral resistance of the pwell, lowering the gain of the pnp transistor, or lowering the operating junction temperature. This is because the npn transistor can be more easily turned on at higher temperatures. The IGBT structure showing the electron injection from the cathode during latch-up, the signature of the latch-up and equivalent circuit to study the latch-up are in the presented below.



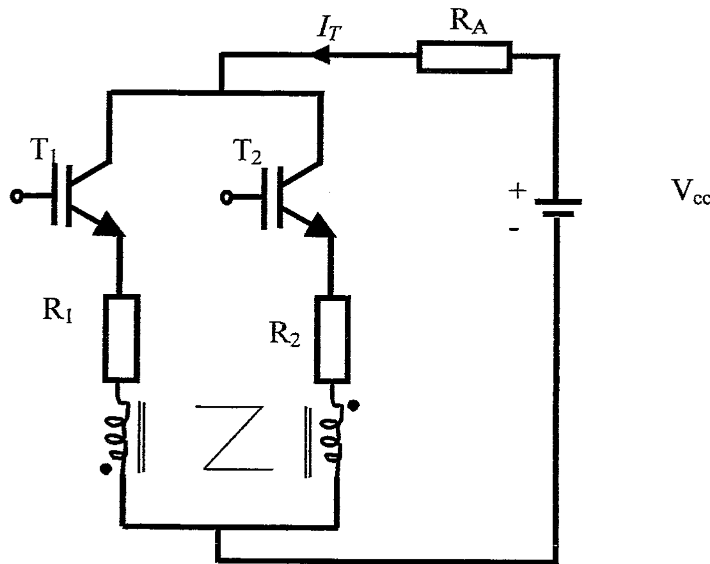
[30%]

b) (i) The resistors R_1 and R_2 introduce a negative feedback which helps the equal sharing of the currents in the two IGBTs in static conditions. There are two main contributions to this negative feedback:

(1) Let us assume that the current in T_1 is higher than in T_2 (imbalance between the two IGBTs). Then the voltage drop across R_1, R_1I_1 is increased. Since $V_{AK1}+ R_1I_1 = V_{AK2} +R_2I_2 =$ const, then V_{AK1} must go down. Given the output characteristics of the IGBT, then the current I_1 must go down (in the linear region, for a given V_{GK}, I_1 is proportional with V_{AK1}) –negative feedback

(2) If the two gates of T_1 and T_2 are connected together to a constant potential V_G, then an increase in the current I_1 results in a higher cathode potential and hence a lower V_{GK} (as V_G is at a constant potential). This results in lowering the I_1 current – negative feedback [20%]

(ii) The dynamic sharing can be accomplished by connecting some small serial inductors in series with the resistors. If the current rises quickly, then *L(di/dt)*, the voltage drop on the inductor increases and hence VDS is forced to decrease (similarly to point (i)). Another solution is to use couple inductors as shown in the next figure. In this case an *L(di/dt)* increase in one of the inductor, would result in a corresponding voltage of opposite polarity induced across the other inductor. As a result the other inductor will take more current – thus rebalancing the current through the two IGBTs, The problem with the inductors is that they can generate spikes and can be quite expansive and bulky.



[20%]

(iii) The sum of the two anode currents, I_1 and I_2 in the IGBTs is equal to the total current I_T.
(1) $I_T = I_1 + I_2$,
According to Kirchhoff:
(2) $V_{AK1} + R_1 I_1 = V_{AK2} + R_2 I_2$

From (1) and (2) $I_1 = (V_{AK1} - V_{AK2} - R_2 I_T)/(R_1 + R_2) = 10.5$ A (52.5%)
$I_2 = 9.5$ A (47.5%)
The imbalance Delta I= 5%

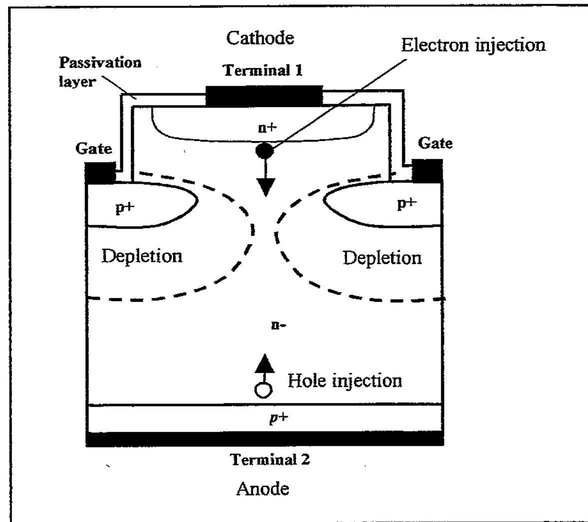
[30%]

Examiner's comment:

This was a popular question. Most of the students answered the theoretical part of the question well but they had problems with calculating the current sharing in the two parallel IGBTs. The last part was slightly more difficult and only a few candidates succeeded in completing it.

3. (a) The structure is a variant of a Static Induction Thyristors (SIT). It is a junction controllable device and comprises a JFET, a diode and a PNP transistor. To obstruct the current flow and turn-off the device, the gate is biased negatively with respect to the cathode to form two depletion regions as shown in the next figure (this is similar to the way the JFET operates). When the two depletion regions meet, the current is pinched off, stopping the injection of electrons from the cathode. However, as opposed to a JFET, here we deal with a bipolar device as the p+ anode layer injects holes (similarly to a PIN diode or the emitter of a PNP transistor)

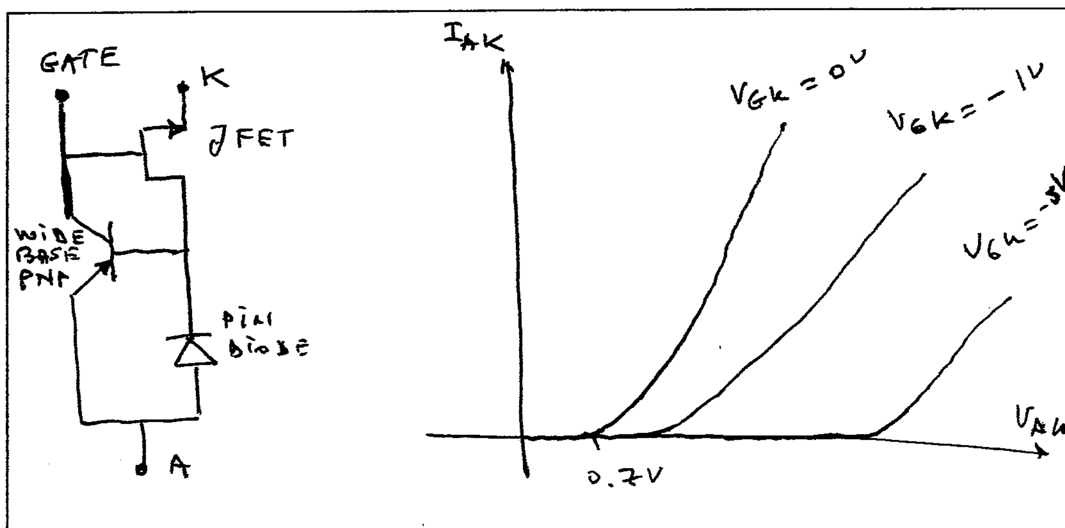
- In the off-state, during the blocking mode, when the anode (TERMINAL 2) is biased at high voltage with respect to the cathode (TERMINAL 1), the voltage is supported in the n-drift region (the p+ layers/n –drift junction is reverse biased and the two depletion regions formed from the p+ meet laterally to pinch the current.
- The device is turned on by removing the negative voltage applied to the gate connected to the p+ layers (or applying a slight positive voltage between the gate and the cathode). As result the depletion region around the p+ layers collapses allowing electron injection from the n+ cathode. This is followed by hole injection from the p+ anode and conductivity modulation.



- In the on-state, there are two bipolar structures which provide the conductivity modulation (and hence the plasma formation) in the drift region, the PIN diode formed between the p+ anode/n-drift and n+ cathode and the PNP transistor formed between the p+ anode as the emitter the n- drift as the base and the p+ gate as the collector. The plasma modulation leads to lowering the resistiance of the n-layer and a superlinear I-V characteristics similar to that of a PIN diode.
- - The turn-off of the device is achieved negatively biased the gate voltage with respect to the cathode potential. As result the depletion region formed around the p+ layers pinch the electron current flow and consequently both the diode and the PNP transitor turn off. The plasma is removed by the depletion sweep of holes to the gate (and eventually a slow recombination process if no lifetime killing is present)

[35%]

(b)

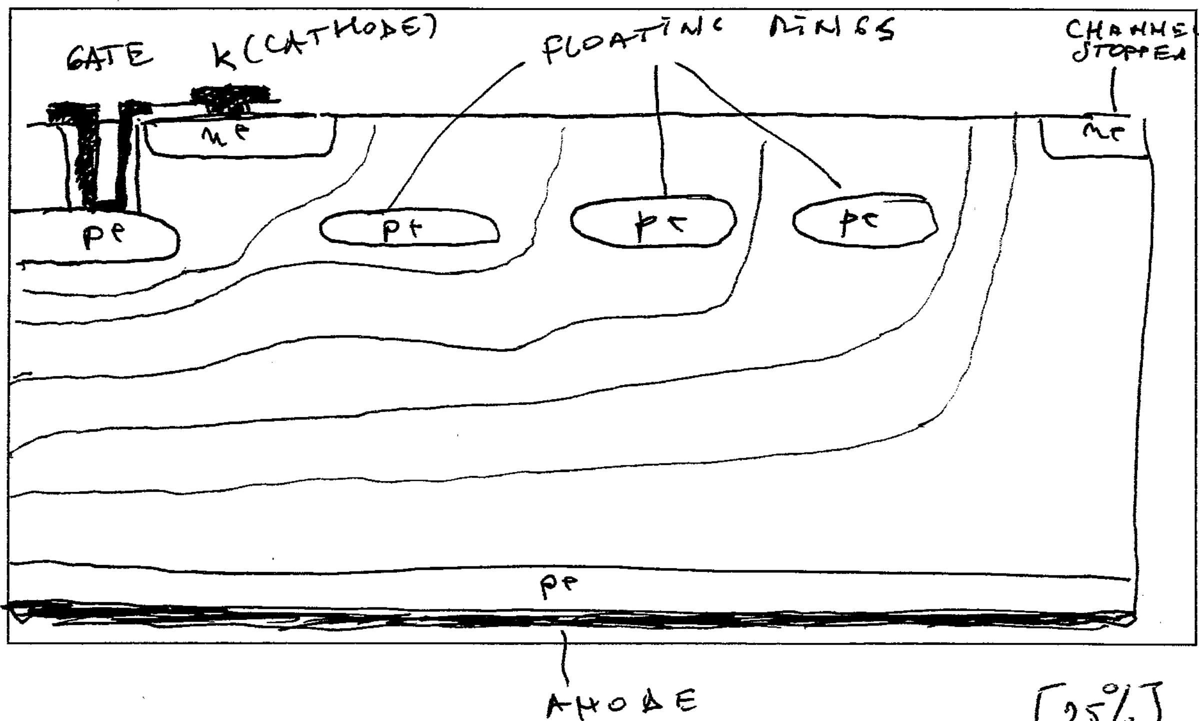


[30%]

(c)

- Advantage: The device has very strong conductivity modulation as it has a double injection – similarly to that in a PIN diode and thyristor. As a result the on-state voltage drop could be smaller than in an equivalent IGBT.
- Disadvantages: The device has no high impedance control (MOS gate). The device also requires negative bias for keeping the device in the off-state, which means more complexity in the drive. [10%]

(d)

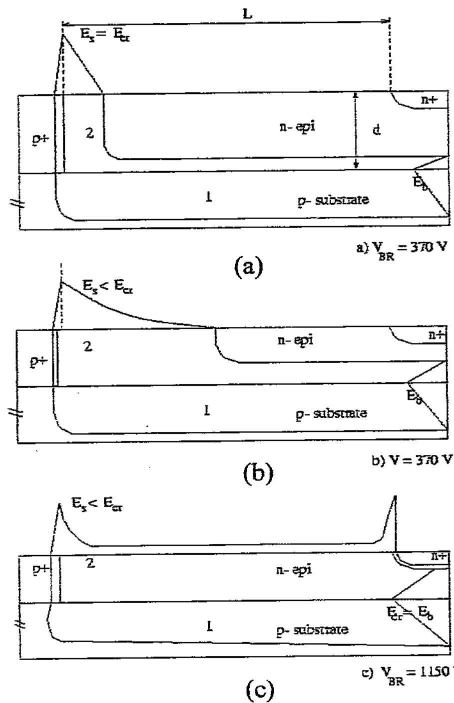


[25%]

Examiner's comments:

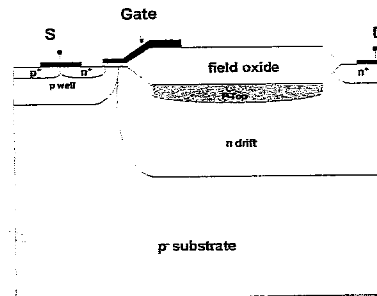
This was quite a popular question but very few candidates managed to work exactly the operation of the device. The undergraduates answered better this question than the graduates.

4. (a) The RESURF effect exploits the meeting of the depletion layers from the horizontal n-epi/p-substrate junction and the n-epi/p well vertical junction to enhance the growth of the depletion layer at the surface. This can be viewed as a more rapid growth of the depletion region than predicted by the 1-D Poisson equation solution for the vertical n-epi/p well junction. Fig (a) on the right shows no interaction between the two depletion regions. Fig. (b) shows that by reducing the n- drift region the two depletions start interacting and the electric field at the surface is lowered. Fig. (c) shows the depletion region and the optimum surface electric field at breakdown. There are three electric field peaks present (two at the surface and one in the bulk at the n- epi/p- substrate junction.

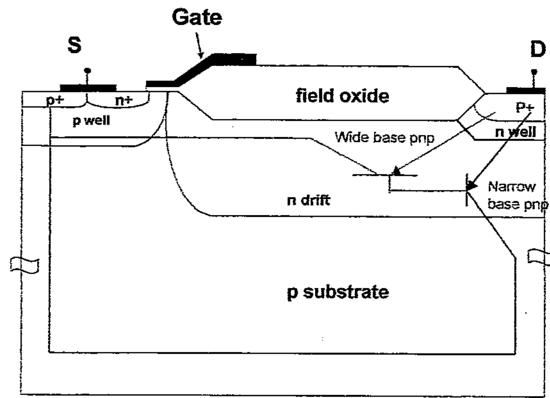


[30%]

(b) The Double RESURF LDMOSFET features an extra p-top at the surface of the device. This is more highly doped than the n-drift region, but is completely depleted at breakdown. Its presence helps further the advance of the depletion region in the n-drift region. As a result the doping of the n- drift region can be increased (almost by 2X) compared to that of a single RESURF device. [20%]



(c) LIGBTs. The structure of the LIGBTs is shown on the right. The presence of the two bipolar elements is indicated.



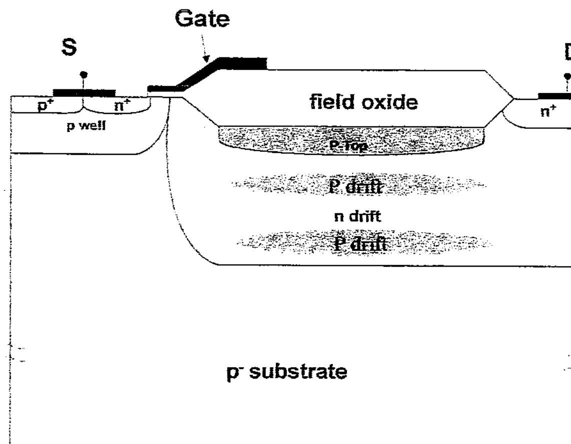
Turn-on: This is similar to the LDMOSFET. The channel induced at the surface of the p well allows flow into the drift region providing that the anode junction is forward biased. The electron current acts as the base current for the pnp transistor leading to injection of holes into the drift region.

On-state: The injection of both holes and electrons into the drift region leads to accumulation of excess mobile carrier charge formed by electrons and holes in equilibrium. As a result the resistance of the drift layer decreases significantly. Note that there are two bipolar transistors (wide-base and narrow base). The narrow base transistor tends to inject plasma deep in the substrate. This transistor is not present in the vertical devices.

Turn-off: The turn-off process is based on sweeping of holes to the cathode short when the depletion advances in the n- drift region from the p well side. Another major turn-off mechanism is via recombination of holes and electrons in the drift region, especially at the anode side where the depletion region takes time to reach. Unfortunately, injection in the on-state does not only occur in the drift region but also in the substrate via the parasitic pnp transistor p+ anode/n-epi/p-substrate. Thus accumulation of parasitic mobile charge occurs deeply in the substrate. This charge has to be removed during turn-off which slows down considerably the turn-off process. Therefore, the turn-off of the LIGBT is generally slow characterized by a specific long tail. As a result the lateral devices can be slower than the vertical devices.

Blocking: This is similar to the LDMOSFET, however in most cases slightly smaller because of the gain of the pnp transistor during avalanche. [30%]

(d) A superjunction in the drift region could be made by adding stripes of p-drift layers between the n-drift layers. These layers are thin and highly doped. In the on-state, the current flows in the n drift stripes between the p layers. Given the high doping of the n drift layers (much higher than in Single and Double RESURF LDMOSFETs), the on-state resistance is decreased.



If charge compensation is achieved, the structure can enhance the breakdown voltage with very low on-state resistance. The electric field at the surface will have almost a rectangular distribution (ideal for power devices). [20%]

Examiner's comments:

In spite of the fact that this was a theoretical question on the RESURF concept, LDMOSFETs & LIGBTs, very few undergraduates and only 3 graduates decided to attempt it. It was generally well answered but there was evidence that this was last answered with some candidates running out of time