PART IIB 2011 PROF G AMARATUNGA

Answers to:
4B14 – Solar electronic power: 2011

Q1. i) Reverse saturation current given as:

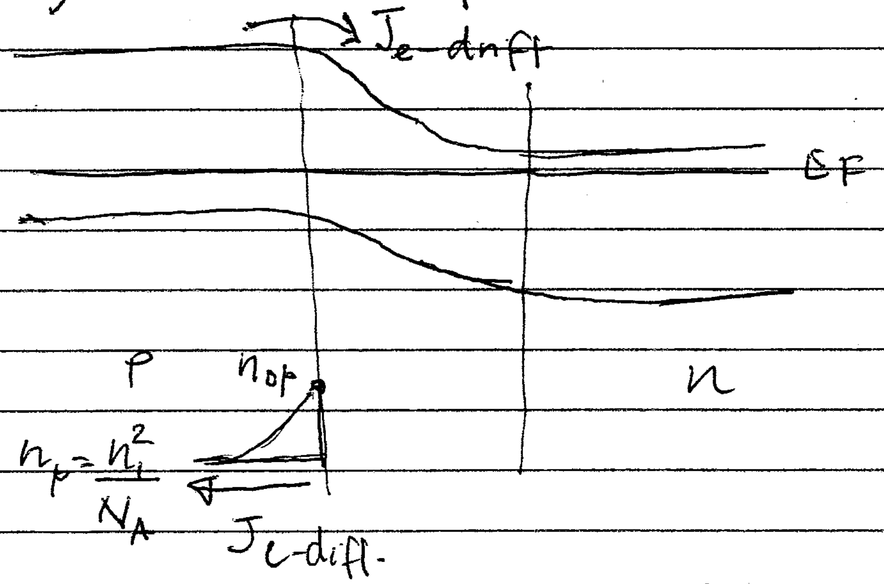
$$I_S = qA\left[\frac{L_e n_i^2}{\tau_e N_A} + \frac{L_h n_i^2}{\tau_h N_D}\right]$$

$$= 1.602\times10^{-19}\times10^{-3}\left[\frac{200\times10^{-6}\times10^{32}}{1\times10^{-6}\times10^{23}} + \frac{0.5\times10^{-6}\times10^{32}}{1\times10^{-9}\times10^{25}}\right]$$

$$= 1.602\times10^{-22}\left[200\times10^{9} + 5\times10^{9}\right]$$

$$= \underline{\underline{32.8\ pA}}$$

ii) Built in potential



At equilibrium (0 bias V), the residual electron current is due to: (i) the minority electrons on the p side which get swept across junction to n-side ($J_{e\text{-drift}}$) and the diffusion electron current on the p-side due the ~~ex~~ electrons thermally excited from the n-side over the barrier.

The total current must however add up to zero at equilibrium: At edge of depletion region of p side:

$J_{e\text{-drift}} + J_{e\text{-diff}} = 0$

$$q n_p \mu_e E + q D_e \frac{dn_p}{dx} = 0$$

$$\therefore \quad E = -\left(\frac{D_e}{\mu}\right)\left(\frac{1}{n_p}\frac{dn_p}{dx}\right)$$

$$E = -\frac{dV_{bi}}{dx} \qquad D_e = \mu_e \frac{kT}{q}$$

$$\therefore \quad \frac{dV_{bi}}{dx} = \frac{kT}{q}\left(\frac{1}{n}\frac{dn}{dx}\right)$$ at all points in the semiconductor

$$\therefore \quad V_{bi} = \frac{kT}{q}\Big[\ln(n)\Big]_{-\infty}^{\infty}$$

$$= \frac{kT}{q}\Big[\ln(n_{\infty}) - \ln(n_{-\infty})\Big]$$

$$= \frac{kT}{q}\left[\ln(N_D) - \ln\left(\frac{n_i^2}{N_A}\right)\right] = \frac{kT}{q}\ln\left[\frac{N_D N_A}{n_i^2}\right]$$

$$V_{bi} = \frac{kT}{q}\ln\left[\frac{N_D N_A}{n_i^2}\right]$$

$$= 0.026 \ln\left[\frac{10^{25} \times 10^{23}}{10^{32}}\right] = 0.026 \ln\left[10^{16}\right]$$

$$= \underline{0.958\ (0.96)\ \text{V}}$$

c) $I = A q D_e \frac{d\Delta n}{dx}$

$\Delta n = \left(n_0 - \frac{N_A}{n_i^2}\right) \exp\left(\frac{-x}{L_e}\right)$

$n_0 - \frac{N_A}{n_i^2} = N_D \exp\left(\frac{(V_A - V_{bi})q}{kT}\right)$

$n_0 - \frac{10^{23}}{10^{32}} = 9.7 \times 10^{18}$

$\boxed{n_0 \simeq 9.7 \times 10^{18}}$

d) $V_{oc} = \frac{q}{kT} \ln\left(\frac{I_{sc}}{I_s} + 1\right)$

$I_{sc} = I_s\left(\exp\left(\frac{0.65q}{kT}\right) - 1\right)$

$\boxed{I_{sc} = 2.36 \text{ A}}$

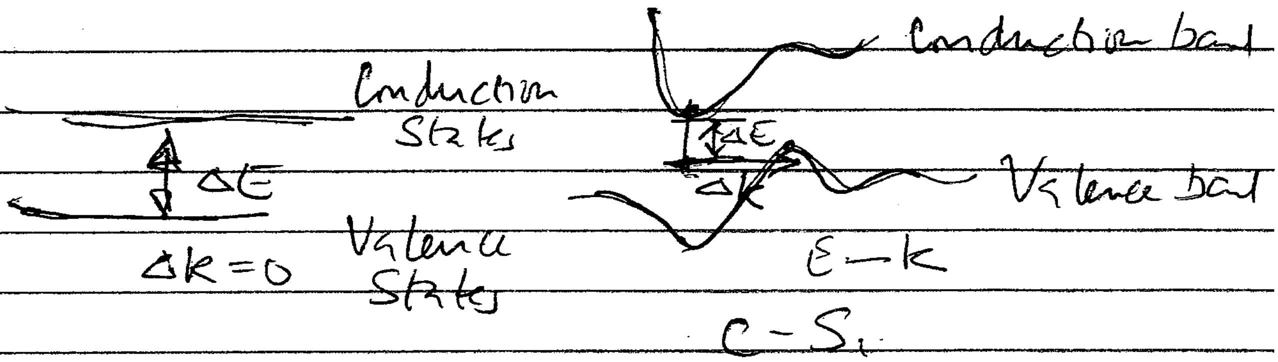
$I_{sc} = q A g_{opt} [L_e + L_h]$

$2.36 = 1.602 \times 10^{-19} \times 10^{-3} \times 200.5 \times 10^{-6} \times g_{opt}$

$\boxed{g_{opt} = 7.35 \times 10^{25} \ s^{-1} m^{-3}}$

Q1 Examiner's Comment: Answered by all students with all except one exhibiting very competent, and many excellent, grasp of the operating principles and the physical phenomena being exploited in a photovoltaic solar cell.

2. a) Amorphous - Si is a pseudo-direct band-gap material as there does not have to be the requirement for conserving momentum ~~for~~ excited electrons from valence band states to conduction band states.
C-Si is an indirect gap material which requires conservation of momentum as electrons are excited into energy states governed by long range crystalline order. Hence a phonon has to be absorbed/generated in order for an energy transition across the gap to occur. This makes photon ~~..~~ absorption (which have no momentum) more difficult.



Hence the same number of photons can be absorbed in a much smaller volume of a-Si:H compared to C-Si

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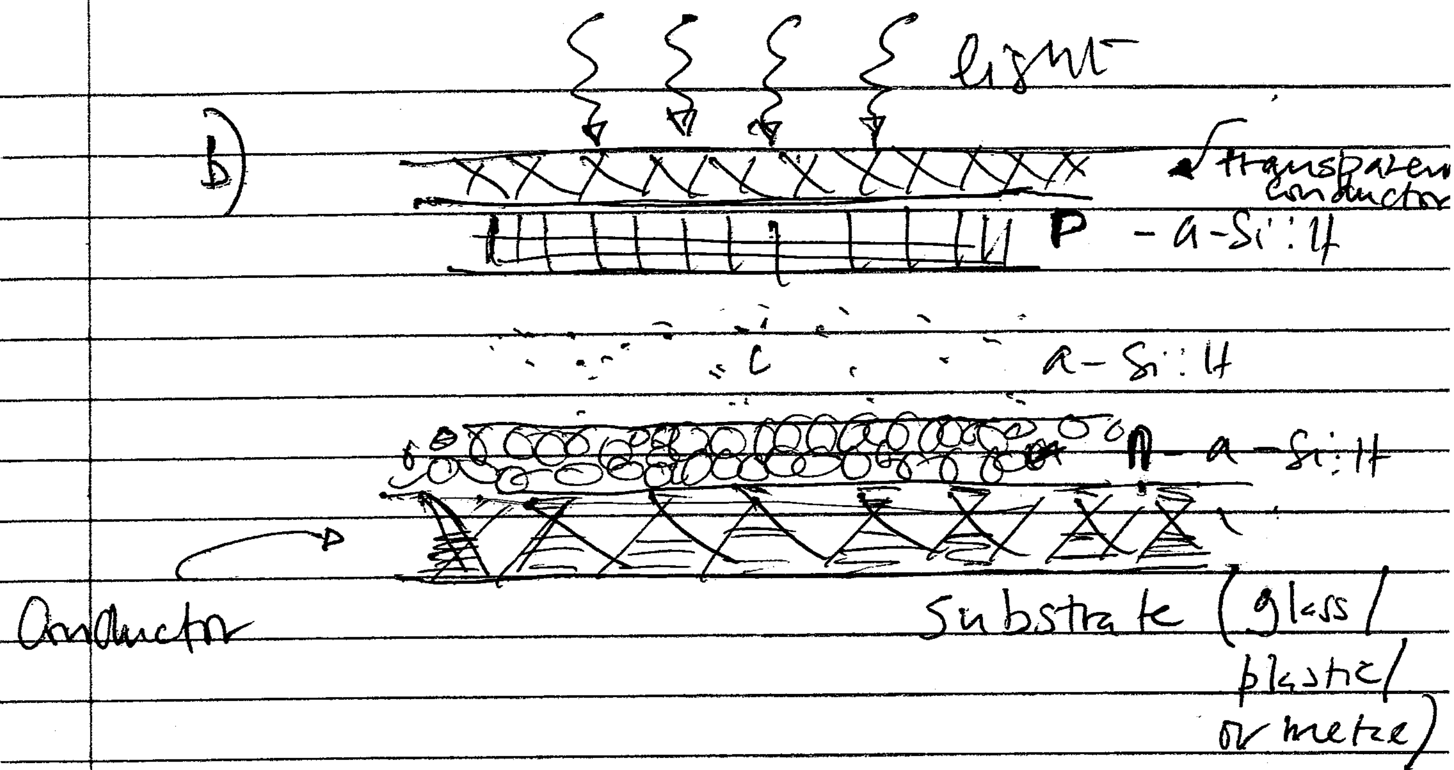
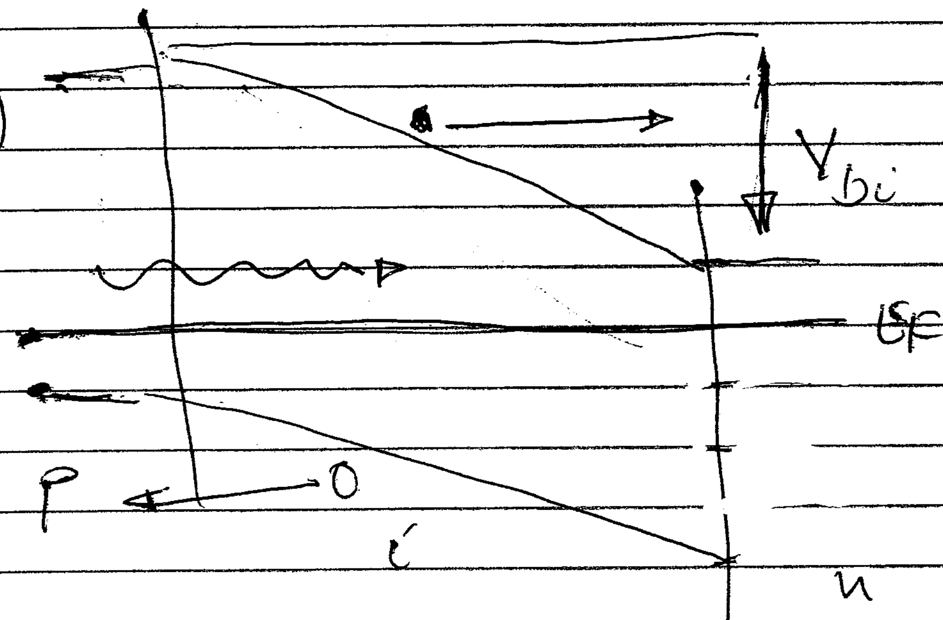
b)



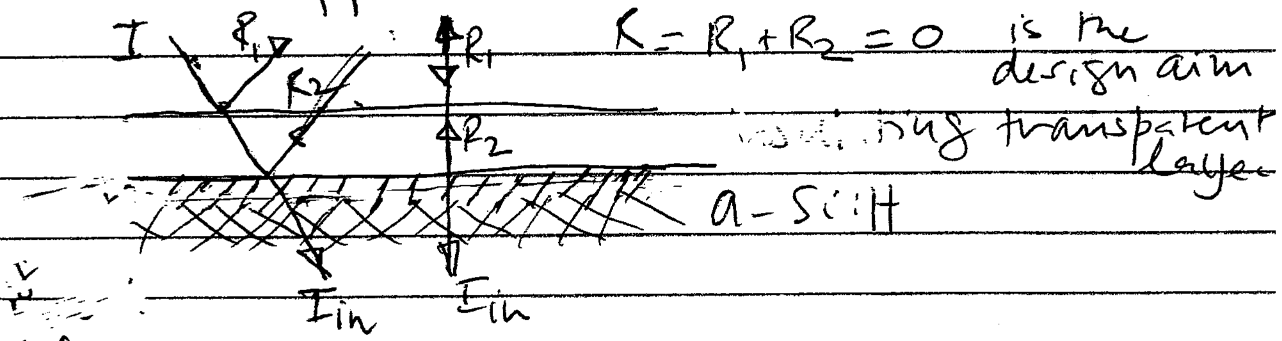
c)



In amorphous semiconductors there are many defect trap states. Therefore the diffusion lengths are very small, of order nanometers. This means photogenerated carriers are unable to diffuse to the junction and be swept across it by the electric field across the depletion region.
Hence, the carriers have to be absorbed

within the depletion region to be subject to the separating electric field due to the built in potential. In order to make the depletion region wide enough to be optimised for maximum photon absorption, it is best to make a intrinsic – a pseudo-insulator – region separating the p and N regions. This intrinsic region then becomes the effective depletion region across which there is a separating electric field to drive electrons and holes in opposite directions before they can recombine or be trapped.

d)



When there is a material interface, such as that between Si and air, there is always some reflection of incident light. It is possible to minimise the reflected light to zero in a given direction of incidence for a particular wavelength by adding an additional material and a second reflective interface.

If the two reflected components of light at a desired wavelength are 180° out of phase then the will cancel each other out. Net result is that all the light enters the Si.

In order to achieve this the thickness of the additional material has to be specifically designed taking into account its refractive index and that of the Si.

e) From the formulae and constants sheet,

$$\theta = \frac{2\pi n_2 d}{\lambda} = \frac{\pi}{2}$$ gives a minimum

reflection condition where d is the thickness of the additional layer and n_2 its refractive index.

$$\therefore d = \frac{\lambda}{n_2 4}$$

Also, $R = 0$ with $n_1 n_3 = n_2^2$ with

$\theta = \pi/2$

$n_1 = 1$ $n_3 = \sqrt{9}$ $\therefore n_2 = \sqrt{3}$

Assume that λ is chosen to minimise reflection at the ~~solar~~ peak of the solar spectrum $\simeq$ 550 nm

$$\therefore d \simeq \frac{550}{\sqrt{3} \times 4} = 79.39 \text{ nm}$$

$$\simeq 80 \text{ nm}$$

The major difference in the optical absorption in amorphous Si compared to crystalline Si was understood by all students. Most also understood the difference in photo-generated carrier transport in the two types of cells as well. The basic concept of the anti-reflection coating was appreciated by all. Most were also able to manipulated the design parameters to achieve zero reflection at a single wavelength.

(Q3)

a) $V_{oc} = \eta \frac{KT}{q} \ln\left(\frac{I_{sc}}{I_s} + 1\right)$

$V_{oc} = 1.1 \times 0.026 \ln(1.5 \times 10^9)$

$= 0.595 \approx \underline{\underline{0.6 V}}$

b) Eff. $\eta = \frac{P_{out}}{P_{in}} = \frac{V_{oc} \times I_{sc} \times FF}{1 \times 10^3 \times 4 \times 10^{-3}}$

FF from formulae sheet, use $FF = FF_0$

$v_o = \frac{q V_{oc}}{\eta K T} = 21$

$FF_0 = \frac{21 - \ln(21 + 0.72)}{21 + 1} = \underline{\underline{0.82}}$

$\therefore$ Eff $= \frac{0.6 \times 1.5 \times 0.82}{4} = \underline{\underline{18\%}}$

(8)

c) $FF = FF_0 (1 - r_s)$

where $r_s = \frac{50 \times 10^{-3}}{(0.6 \times 1.5)} = 0.125$

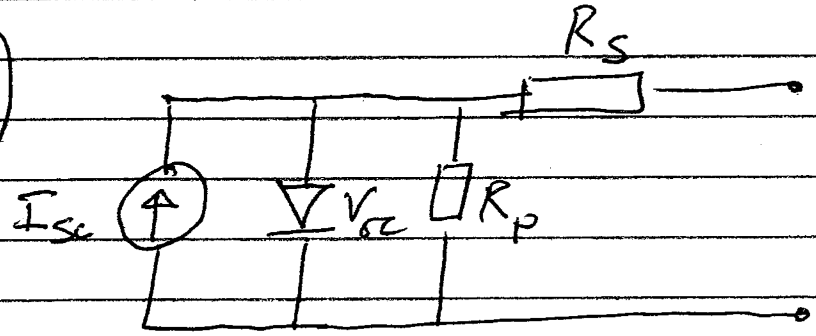
$\therefore FF = 0.82 \times 0.875 = 0.7175$

$\underline{\underline{0.72}}$

$\therefore$ new efficiency $= 0.18 \times 0.875$

$= 0.16 = \underline{\underline{16\%}}$

d)



I_{SC} = ideal short circuit current

V_{OC} = " Open Circuit Voltage

R_s = Series resistance with junction due to bulk semiconductor and contact resistance

R_p = Parallel resistance with junction. This is the leakage path across junction, mainly at the perimeter edge.

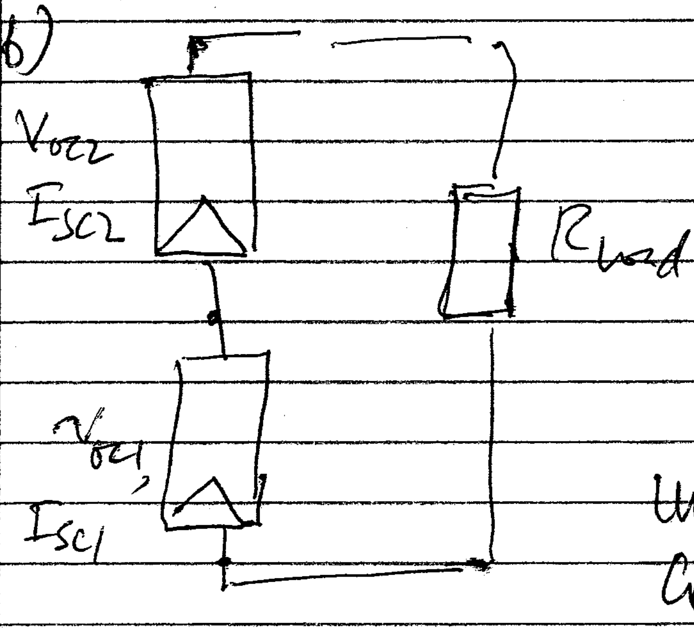
Q3 Examiner's comment: Solar cell efficiency calculation was well understood. The finer points of efficiency limitation in solar cells were also appreciated. Modelling a cell using an equivalent circuit was also handled competently.

Q4

(a) A solar cell has an open circuit voltage below 1V. This is governed by the basic physics of the photovoltaic conversion process with sunlight and a semiconductor junction.

A sub 1V V_{oc} is not practice for direct connection to any significant power extraction circuit/system. Therefore cells connected in series to obtain a voltage suitable for connection into a power extraction system. Typically cells assembled in a module to have a module open circuit voltage of 24 - 60V.

(b)



$$V_{oc1} = \frac{KT}{q} \ln\left(\frac{I_{sc1}}{I_{s1}} + 1\right)$$

$$V_{oc2} = \frac{KT}{q} \ln\left(\frac{I_{sc2}}{I_{s2}} + 1\right)$$

Under short circuit conditions, i.e $R_{load} = 0$

$$V_{c1} + V_{c2} = 0$$

$\therefore$ $V_{c1} = -V_{c2}$ and $I_{SC-mod} = I_1 = I_2$

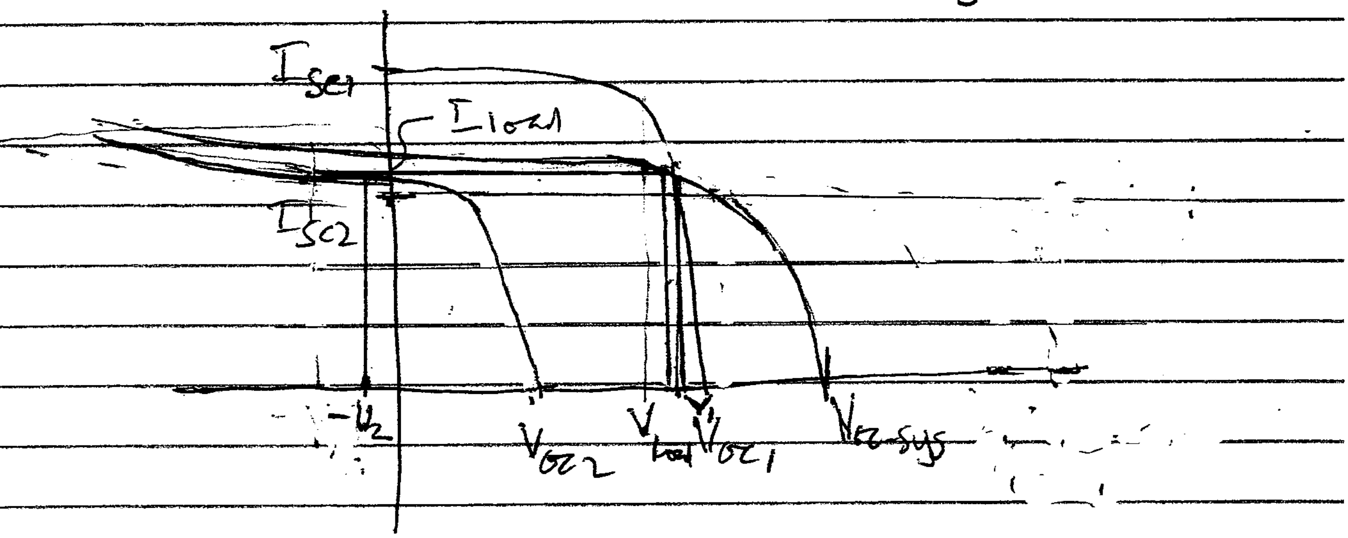
$$I_1 = I_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right] - I_{sc1} \quad (1)$$

$$I_2 = I_s\left[\exp\left(\frac{-qV_1}{kT}\right) - 1\right] - I_{sc2} \quad (2)$$

$\therefore \; I_1 = I_2$

$$0 = \exp\left(\frac{qV}{kT}\right) - \exp\left(\frac{-qV_1}{kT}\right) - I_{sc1} + I_{sc2}$$

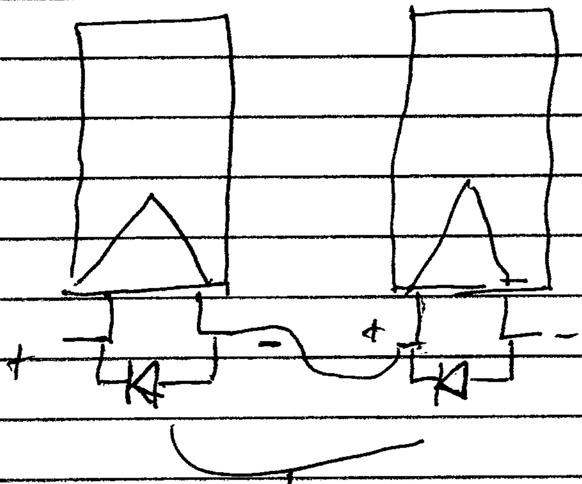
$$\therefore \; V_1 = \frac{kT}{e}\sinh^{-1}\left(\frac{I_{sc1} - I_{sc2}}{2I_s}\right)$$



Therefore unless $I_{sc1} = I_{sc2}$ and $V_1 = V_2 = 0$ power can be dissipated through operation in the 3rd quadrant (i.e. $-V$, $-I$, VI +ve and power dissipated)

~~(c) By having a by-pass diode~~

So that when the voltage across a module becomes negative, it is shorted out/bypassed



by pass diodes.

Advantages

(d) Microinverters allow the optimum power available from each module to be connected to the AC grid. Maximum power point individually for each module. There are no by-pass diodes. Each module is in effect <u>parallel</u> connected to the grid.

This allows more <u>energy</u> harvest over time.

Disadvantages

Because each module handling smaller power, the efficiency is 1-2% less. (12)

More costly per Watt – more electronics

String inverters – 1kW min rating, efficiency higher. Less cost.

(e) Domestic DC grid being proposed to support LED lighting (more efficient. Additionally Electric Vehicle charging in houses proposed. So in theory a DC grid would also help this. But DC voltages ~~and~~ for EV charging and LED lighting may not be the same. If a common Bus voltage can be standardized, then solar modules can be ~~[illegible]~~ designed to have same nominal output voltage.

The voltage/power conditioning will then be only $DC_{solar} - DC_{bus}$, $DC_{bus} - DC_{LED}$, $DC_{bus} - DC_{EV}$. There is no AC – DC or DC – AC conversion steps in between. Therefore system should be more efficient.

It seems this year the students preferred the cell level questions to the one which covered cell assembly into modules and the power electronic aspects for grid connection. This may also be because 35% of the available marks were associated with writing a commentary on the suitability of a 'PV backed domestic DC grid for lighting and electric vehicle charging'. This was not specifically covered in the lectures, but relied on the candidate's general reading and expanded thinking. Not a good idea!