ENGINEERING TRIPOS PART IIB

Friday 29 April 2011 2.30 to 4.00

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. Consider the circuit of Fig. 1, in which an NMOS transistor *M1* is connected in a circuit designed to provide a reference voltage V_{REF}.

(a) Derive an expression relating V_{REF} with the drain current I, transistor parameters and other circuit constants. [20%]

(b) The transistor dimensions W and L are chosen as 40 μm and 4 μm respectively, V_{DD} and V_{SS} are 6 V and 0 V respectively, and other transistor parameters for *M1* are as follows:

$V_T = +1$ V, and $\mu_N \varepsilon / t_{OX} = 20 \times 10^{-6}$ AV^{-2}

Deduce a suitable value for R if V_{REF} is to be 2 V, and determine the drain current I. [20%]

You may assume the following expressions for the drain current I_D in a MOS transistor.

$$I_D = \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \qquad 0 < V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{1}{2} \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} (V_{GS} - V_T)^2 \qquad 0 < V_{GS} - V_T < V_{DS}$$

(c) What is meant by the following terms in the context of the performance of voltage references, and why are they important?

(i) Power supply sensitivity

(ii) Fractional temperature coefficient [20%]

(d) Write a short account of the approaches available to the CMOS IC designer for generating stable reference voltages for use in integrated circuit designs. Your account should mention power consumption, stability, area occupied, and any other factors you consider to be important. [40%]

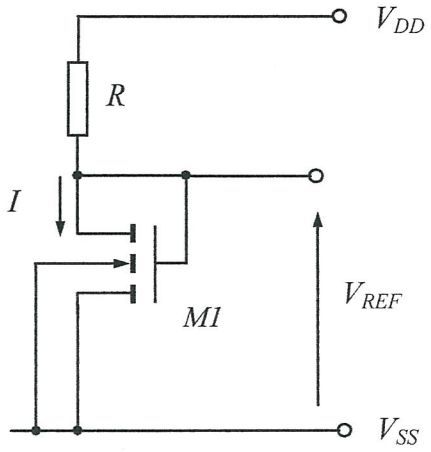

Fig. 1

2. (a) Sketch and annotate the cross-section of a n- and p-channel pair of metal oxide semiconductor field effect transistors on p-type silicon as the elementary building block of CMOS technology. [20%]

(b) List, in order, the processing steps required to make such a pair, adding comments on the reasons for the order of the processing steps. [40%]

(c) What is the reason for going to a silicon-on-insulator technology (SOIT)? Describe three different realisations of SOIT. [40%]

3. (a) Discuss the practical importance of quality assurance regimes in the production of VLSI circuits. [20%]

(b) Describe five different forms of stress that a high-performance VLSI chip can endure during its operation, how those stresses can limit product lifetime, and what measures during manufacture can be used to mitigate these stresses. [40%]

(c) Discuss the various failure mechanisms that together result in the bath-tub curve as used to describe the failure of VLSI products. [40%]

4. (a) Describe the primary causes of dissipation of electrical power in a CMOS digital integrated circuit, indicating the circumstances and classes of circuits in which they are dominant. [25%]

(b) What are the means available to the IC designer to reduce the energy consumption of a full-custom CMOS digital integrated circuit? In your account you should refer to process and device selection, as well as any circuit techniques and abstractions in which economy of power may be optimised. [30%]

(c) In a multimedia application, the input data-path of a stream-based digital multimedia processor is implemented as an integrated module using a 0.7 μm CMOS process. This module may be modelled as a large array of 36,000 memory elements, organised as a set of eighteen 2,000-bit shift registers. Binary data sequences are accepted at eighteen input pins, and are applied to the serial inputs of the shift registers. The shift registers operate continuously, clocking data serially from input to output and are driven with a 100 MHz clock to all stages. On appearing at the serial outputs, the data patterns are presented to the processor itself.

Each memory element drives a load which may be assumed to be purely capacitive and equivalent to 15 fF. By considering the dynamic power dissipated in the array as data are clocked through, estimate the worst-case current consumption of that part of the circuit, assuming that the supply V_{DD} is 3.3 V. For this calculation you may ignore power losses due to other mechanisms. State any other assumptions made. [25%]

(d) Discuss briefly the potential inaccuracies introduced in (c) by neglecting losses from other sources. The processor described is to be adapted for an application in which power consumption must be minimised. Briefly outline the options available to the designer to achieve this. [20%]

5. (a) Describe the circuit and mode of operation of a transmission gate in complementary MOS technology, and explain clearly how this circuit may provide performance superior to that of a simple pass transistor. Give examples of the use of transmission gates in:

(i) digital circuits

(ii) analogue circuits,

briefly indicating any advantages and disadvantages of the circuit in these applications. [50%]

(b) What are the critical success factors for VLSI manufacture? [25%]

(c) What considerations apply to the physical layout of a VLSI production line? [25%]

END OF PAPER