## ENGINEERING TRIPOS PART IIB 2012
## 4M6 MATERIALS AND PROCESSES FOR MICROSYSTEMS (MEMS)

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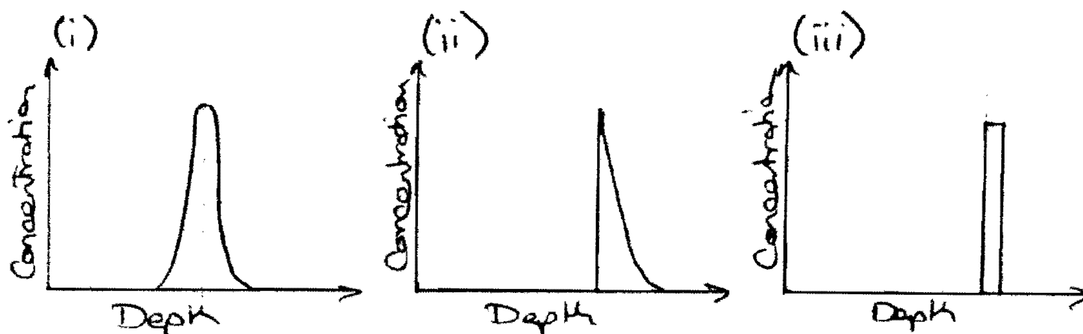
1 (a) (i) Ion implantation allows a layer of an impurity atom to be created a particular depth below the surface of a crystalline silicon wafer. The precise depth is controlled by the kinetic energy of the ions, and this is well characterised. The concentration profile is shown below. The advantage of this process is that only one step – the ion implantation – followed by a simple anneal is required. However, the concentration will follow a Gaussian distribution with depth. Therefore, it will not be possible to precisely define where the etch will stop.

(ii) Impurity diffusion involves exposing the surface of a silicon wafer to a supply of impurity atoms from a gaseous precursor. The surface of the wafer is saturated in the impurity and an elevated temperature allows the impurity to diffuse into the bulk. However, this occurs at the surface of the wafer. Therefore, to produce a buried layer will require growth of crystalline silicon over the impurity layer after diffusion by molecular beam epitaxy. This is slow and costly, but there will be a good step change in impurity concentration with depth on the upper surface of the impurity layer, as required, and as shown below.




(iii) Molecular beam epitaxy can be used alone by introducing the impurity into the MBE system during growth. This would be employed initially to grow the layer with the impurity before the impurity supply is turned off and pure crystalline silicon growth continues. This would again precisely define the doped region with depth, as shown below, but it would be slow and costly.

(b) From Fig. 1, a 500 nm implantation depth will require the use of <u>200 keV ions</u>.

We now require the dose. We should want the etch rate to drop by ~99%, so this requires a relative etch rate of $10^{-2}$. This means a peak boron concentration of $10^{26}$ m$^{-3}$ from Fig. 2. From the Data Book,

$$N_i(x) = \frac{Q_i}{\Delta R_p \sqrt{2\pi}} \exp\left[\frac{-1}{2}\left(\frac{x - R_P}{\Delta R_P}\right)^2\right]$$

However, the peak value occurs when $x = R_P$, so this reduces to

$$N_i(R_P) = \frac{Q_i}{\Delta R_p \sqrt{2\pi}}$$

Hence,

$$Q_i = N_i \Delta R_P \sqrt{2\pi}$$

From Fig. 2, at 200 keV, $\Delta R_P = 0.09$ μm, so

$$Q_i = 10^{26} \times 0.09 \times 10^{-6} \sqrt{2\pi} = \underline{2.26 \times 10^{19} \text{ m}^{-2}}$$

(c) We can calculate, using the formula in the Data Book and the answer to part (b), the impurity concentration 50 nm above the desired implantation depth as

$$N_i(x) = \frac{Q_i}{\Delta R_p \sqrt{2\pi}} \exp\left[\frac{-1}{2}\left(\frac{x - R_P}{\Delta R_P}\right)^2\right]$$

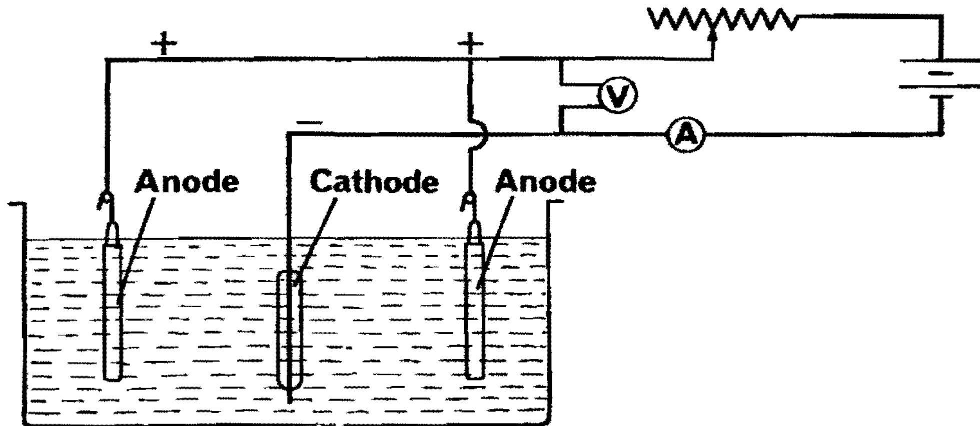
$$N_i(x - R_P = 50 \text{ nm}) = \frac{2.26 \times 10^{19}}{0.09 \times 10^{-6} \sqrt{2\pi}} \exp\left[\frac{-1}{2}\left(\frac{50 \times 10^{-9}}{0.09 \times 10^{-6}}\right)^2\right] = 8.6 \times 10^{25} \text{ m}^{-3}$$

From Fig. 2, the relative etch rate is still only ~0.015, and so the etch is very slow and the desired tolerance has not been achieved.

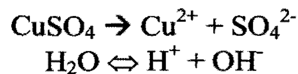
**Examiner's comment:**

This question examined the students' understanding of methodologies for producing buried dopant layers in crystalline silicon to produce an etch stop. Whilst most candidates performed a good calculation of required dopant dose by ion implantation, only a minority were able to integrate molecular beam epitaxy with dopant diffusion to achieve an improved etch stop layer.

2 (a) Electroplating is the application of metallic coatings to conductive surfaces by electrochemical processes. The sample to be coated, which must have a conductive surface, is placed in a solution of the metal salt to be deposited together with another conducting plate and these are connected as the cathode and anode respectively to a low voltage, dc power supply. In aqueous solution, the metal salt will dissociate, as will the water to a small extent.



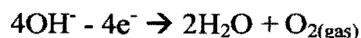

For example, for the plating of copper using copper sulphate,



$$CuSO_4 \rightarrow Cu^{2+} + SO_4^{2-}$$
$$H_2O \Leftrightarrow H^+ + OH^-$$

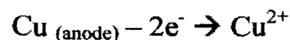
Under the application of a bias to the electrodes, the positive ions will migrate to the cathode. The metal ions will be deposited onto the electrode surface while the $H^+$ ions will mostly react to form gaseous hydrogen, although a small quantity may be incorporated into the metal. The reaction at the anode will depend on its nature.

For an inert anode, the hydroxyl ions will be discharged,



$$4OH^- - 4e^- \rightarrow 2H_2O + O_{2(gas)}$$

As the anode is inert, the salt ions cannot react and so are not discharged. This has the disadvantage that the metal ion is depleted from the solution with time. Alternatively, the anode may be made from the depositing metal, in which case it will be dissolved into the solution in preference to any other electrochemical reactions at low voltages. For example, the reaction at a copper anode will be



$$Cu_{(anode)} - 2e^- \rightarrow Cu^{2+}$$

(b) Thick photoresists, such as SU8, can be formed in layers with thicknesses ~100 μm. However, they can be patteren with high lateral resolution (~1 μm) like normal photoresists. Careful development allows highly vertical sidewalls to be realised. In this way deep trenches can be produced in the photoresist which extend down through the entire photoresist thickness to the substrate. If such structures are patterned onto a conducting surface, then electroplating can subsequently be applied. As the photoresist is insulating, no deposition will occur on the photoresist surface. However, the exposed substrate will be coated. The deposition will then be restricted to the trench, which will be filled with metal. After electroplating, the photoresist can be selectively etched to leave a high aspect ratio metal structure.

(c) (i) The process flow is as follows:

| *Step* | *Code* | *Description* |
|---|---|---|
| 1 | RCA1 | Boil the oxide-coated silicon substrate in RCA Clean 1 ($NH_3$(aq):$H_2O$:$H_2O_2$) to remove organic contaminants. |
| 2 | RCA2 | Boil the oxide-coated silicon substrate in RCA Clean 2 (HCl:$H_2O$:$H_2O_2$) to remove metallic ion contaminants. |
| 3 | SPU1 | Sputter deposit a thin film of chromium (~10 nm) onto the wafer to act as a conduction path for electroplating. |
| 4 | PHO1 | Spin a layer of SU8 photoresist onto the silicon wafer. |
| 5 | BAK1 | Pre-bake the photoresist. |
| 6 | EXP1 | Expose the photoresist through a mask to produce a pattern in the photoresist which will form a series of 10 μm diameter holes where the Cu pillars will be. |
| 7 | DEV1 | Develop the photoresist. |
| 8 | BAK2 | Post-bake the photoresist to harden it. |
| 9 | ELP1 | Electroplate copper into the holes using copper sulphate solution. |
| 10 | DIW1 | Rinse in DI water and blow dry. |
| 11 | RIE1 | Use an $O_2$ plasma ash etch to selectively remove the SU8. |
| 12 | IWE1 | Use an isotropic wet etch of chromium to remove the exposed seed layer. |
| 13 | DIW2 | Rinse in DI water and blow dry. |

(ii) The mass of metal per unit area per unit time deposited is given by (from the Data Book)

$$M = \frac{JA}{zF}$$

Hence, this can be related to density and deposition rate by $\rho = M/R$ giving

$$J = \frac{R\rho zF}{A}$$

For the 60 μm pillars to be filled in 20 minutes requires a deposition rate of 50 nm $s^{-1}$. The density of copper is 8940 kg $m^{-3}$, its valency is 2 and its atomic weight is 63.54amu. Therefore, if the Faraday constant (from the Data Book) is 96500 C, the current density if we were coating the whole area would be

$$J = \frac{R\rho zF}{A}$$

$$J = \frac{50\times10^{-9}\times8940\times10^{3}\times2\times96500}{63.54}$$

$$\underline{J = 1357\ \text{A m}^{-2}}$$

However, in reality, we are only coating a fraction of the area where we have holes, which is

$$\text{Area fraction} = \frac{\pi\left(5\times10^{-6}\right)^2}{\left(100\times10^{-6}\right)^2} = 7.8\times10^{-3}$$

Therefore, the actual current density is

$$J = 1357\times7.8\times10^{-3}$$

$$\underline{J = 10.66\ \text{A m}^{-2}}$$

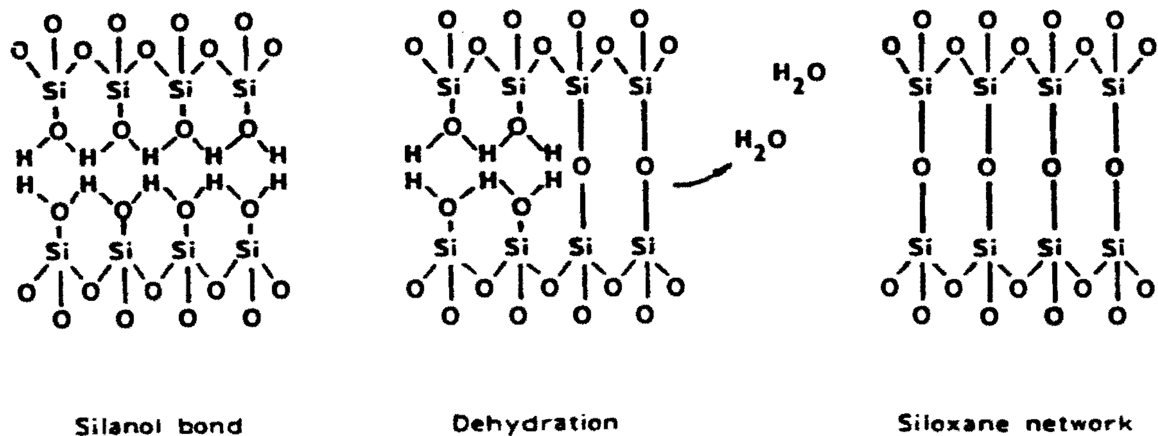
Examiner's comment:

**This question examined the students' understanding of the method of electroplating in general and then specifically high aspect ratio structures. A short process flow was then required with a calculation of plating currents. Both process flow and calculation were well attempted.**

3 (a) The direct bonding of two silicon wafers occurs by a three step process.

The first step is wafer preparation. Initially the surfaces of the two wafers must be prepared for mating. Both surfaces must be cleaned and hydrophilised so that water molecules chemisorb onto the two surfaces. This is normally achieved by wet cleaning followed by a dry plasma hydrophilisation. A major concern in all bonding processes is the presence of voids caused by non-contacting areas due to particles, organic residues, surface defects and inadequate mating. Aligned mating must be performed in a particle free environment with good control of the mechanical contact (which is complicated surface patterns)

The second step is wafer fusion. The two wafers are then brought into mechanical contact and adhere via hydrogen bridge bonds between the surface water molecules. Natural wafer bow normally allows contact to be initiated in the centre of the wafer from where it spreads out radially.




The final step is annealing. Post-fusion annealing is required to increase the strength of the bond by causing the water molecules on the internal surface to form Si—O—Si bridge bonds. Ideally, a temperature of above 1000° C applied for several hours should be used to ensure maximum bond strength.

(b) Optimum bond strength may not be achieved for a number of reasons. A very common problem is the presence of features on the wafer (which is frequently inevitable in real device fabrication). The features disrupt the fusion process leading to voids between the two wafers reducing contact area and hence bond strength. Another common factor is the need to limit the annealing temperature. In general, the bonding strength increases with annealing temperature, and it is normally the presence of other materials which limits the temperature employed. Metallised wafers cannot normally be heated above 450° C otherwise the metal may melt. Diffusion or implantation doped wafers cannot normally be heated above 800° C without allowing further unwanted dopant migration.

(c) The process flow is as follows:

| *Step* | *Code* | *Description* |
|---|---|---|
| 1 | RCA1 | Boil three silicon substrates in RCA Clean 1 ($NH_3(aq):H_2O:H_2O_2$) to remove organic contaminants. |
| 2 | RCA2 | Boil the three silicon substrates in RCA Clean 2 ($HCl:H_2O:H_2O_2$) to remove metallic ion contaminants. |
| 3 | SIO1 | Deposit 200 nm of silicon dioxide by rf-PECVD onto one side of all three silicon wafers. |
| 4 | PHO1 | Spin a layer of AZ5214E photoresist onto the two of the silicon wafers. |
| 5 | BAK1 | Pre-bake the photoresist. |
| 6 | EXP1 | Expose the photoresist through a mask to produce a pattern in the photoresist which will form a series of 350 μm diameter holes which will form where the cavities are. |
| 7 | DEV1 | Develop the photoresist. |
| 8 | BAK2 | Post-bake the photoresist to harden it. |
| 9 | BHF1 | Etch the exposed silicon oxide with buffered HF acid. |
| 10 | DIW2 | Rinse the wafers with DI water and blow dry. |
| 11 | ACE1 | Ultrasound wafers in acetone to remove the photoresist. |
| 12 | ISO1 | Ultrasound wafers in isopropanol to remove the acetone. |
| 13 | DIW1 | Ultrasound wafers in DI water and blow dry. |
| 14 | DRI1 | Deep reactive ion etch into the exposed silicon to a depth of 10 μm to form part of the cavities. |
| 15 | BHF1 | Remove the remaining silicon oxide with a buffered HF acid etch. |
| 16 | DIW3 | Rinse the wafers with DI water and blow dry. |
| 17 | SIN1 | Deposit 5 μm of silicon nitride by rf-PECVD onto one side uncoated of the third silicon wafer. |
| 18 | PHO1 | Spin a layer of AZ5214E photoresist onto the oxide coated side of the silicon wafer. |
| 19 | BAK1 | Pre-bake the photoresist. |
| 20 | EXP1 | Expose the photoresist through a mask to produce a pattern in the photoresist which will form a series of 350 μm diameter ring doughnut shapes with a 250 μm inner region which will form the proof masses and surrounding cavities. |
| 21 | DEV1 | Develop the photoresist. |
| 22 | BAK2 | Post-bake the photoresist to harden it. |
| 23 | BHF1 | Etch the exposed silicon oxide with buffered HF acid. |
| 24 | DIW2 | Rinse the wafers with DI water and blow dry. |
| 25 | DRI1 | Deep reactive ion etch into the exposed silicon through to the silicon nitride on the reverse side. |
| 26 | BHF1 | Remove the remaining silicon oxide with a buffered HF acid etch. |
| 27 | DIW3 | Rinse the wafers with DI water and blow dry. |
| 28 | ANN1 | Anneal the silicon nitride wafer at 1000 °C to dehydrogenate. |
| 29 | FUS1 | Fusion bond the three wafers together. |
| 30 | ANN1 | Anneal the wafers at 1000 °C to strengthen. |

**Examiner's comment:**

This question examined the students' understanding of direct fusion bonding of wafers and the application of this in a process flow for the fabrication of a MEMS accelerometer. Whilst there were a few excellent process flows, many students made this unnecessarily complicated by attempting to use only two wafers, rather than three, leading to very complicated and inaccurate flows.

4 (a) Yield is a measure of the number of devices or component parts produced versus the expected number given the amount of incoming materials and devices processed. In the practical fabrication of a MEMS device, many devices will be fabricated simultaneously on a single substrate. Therefore, if a number of substrates are being processed, the total number of devices that are being fabricated is the multiple of the number of wafers processed and the number of devices per wafer. Each step in the process flow will have a yield (one can imagine a particular process step causing a few devices on a wafer to fail or a whole wafer of devices to occasionally fail, however a simple yield percentage will not distinguish between these). Therefore, only a fraction of the total number of devices that are being fabricated will actually operate, and this fraction is the yield.

(b) The overall yield is given by

$$0.80 = 0.95^2 \times x^{18}$$
$$x^{18} = 0.886$$
$$18 \lg x = \lg(0.886)$$
$$\lg x = \frac{-0.0524}{18}$$
$$\underline{x = 0.993}$$

(c) (i) Stiction occurs when some force causes the mechanical collapse of a suspended structure. Such forces include electrostatic forces, capilliary forces and shock loads. Adhesion then occurs between the two solid surfaces in contact in a similar process to wafer bonding due to the elimination of a surface, thereby gaining energy, and there being insufficient mechanical energy to restore the system. The high surface to volume ratio in MEMS devices makes then particularly susceptible to stiction.

In the case of electrostatic pull-in, consider a beam suspended over a substrate with an air gap g between the two. If there is a potential difference between the beam and the substrate, then there will be an electrostatic force which will tend to pull the beam down, but this will resisted by a restoring elastic force. As the restoring force only scales linearly with the gap, whereas the electrostatic force scales as gap$^{-2}$, there is only a finite region of stability. Hence, if the voltage increases above a critical 'pull-in' voltage, or the gap decreases below a critical 'pull-in' gap, then the elastic force cannot balance the electrostatic force, and the structure collapses.

Capillary forces can cause the collapse of suspended structures after a sacrificial wet etch or even during normal operation of a device in a humid environment (such as an autoclave). Increasing the surface area of a liquid requires work – the surface tension. For a suspended stricture above substrate, a quantity of liquid will exist in the gap region

between the two. The liquid will attempt to minimise its surface area with the air by minimising the gap, and will attempt to pull down the suspended structure. If the surface energy gain exceeds the elastic energy cost, then collapse will occur.

Finally, the application of a sudden acceleration (a shock) to a suspended structure may, when the time period of the shock is of the order of the time period for resonant oscillations in the suspended structure, cause the structure to move into contact with the substrate. Once again, if the energy gain by removing the surfaces between the suspended structure and the substrate exceeds the elastic energy cost, then the suspended structure will be permanently adhered to the substrate.

(ii) Three methods for reducing the likelihood of stiction are:

- Change the geometry of the suspended structure to increase the elastic energy relative to the surface energy gain by stiction (increased thickness, increased gap, reduced free length)
- Texture the underside of the suspended structure or the top side of the substrate so that if contact occurs, only a very small area is actually in contact and so the surface energy gain is very small.
- Apply a low surface energy coating between the underside of the free-standing structure and surface of the substrate (such as a self-assembled monolayer or diamond-like carbon).

(d) Other factors that lead to poor yield include:

- Quality of interfaces, and particulary at points of bonds and interconnects
- Stress which can deform and break a structure including residual stress and stress gradients
- Particle contamination
- Fracture
- Gross errors including incorrect tool settings
- Packaging

Examiner's comment:

This question examined the students' understanding of the issue of yield in the fabrication of MEMS devices with an emphasis on yield. Answers given tended to be of a rather cursory nature for the description of yield with specific relation to MEMS, but descriptions of stiction were of a generally high standard.