ENGINEERING TRIPOS PART IIB

Wednesday 9 May 2012 2.30 to 4

Module 4B6

SOLID STATE DEVICES AND CHEMICAL/BIOLOGICAL SENSORS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachment: Formulae and Constants sheet (1 page)

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Define the threshold voltage for a MOSFET. [20%]

(b) Calculate the threshold voltage for a silicon n-MOSFET with the following parameters:

gate oxide thickness	$d=1.0\times10^{-8}$ m
oxide dielectric constant	$\varepsilon_i=3.9\ \varepsilon_0$
semiconductor dielectric constant	$\varepsilon_S=11.9\ \varepsilon_0$
acceptor concentration	$N_A= 1.0\times10^{21}\ m^{-3}$

Assume the device is ideal and V_{DS} is negligibly small. [40%]

(c) n-channel MOSFETs with the above parameters are fabricated and, due to a fault in the process, some fixed charge is present at the oxide/semiconductor interface.

From the I_D-V_{GS} data below, obtained for V_{DS}=0.001 V, determine the density and sign of the fixed charge.

V_{GS} (V)	I_D (A)
1.0	$1.43\text{x}10^{-6}$
1.4	$1.89\text{x}10^{-6}$
1.8	$2.35\text{x}10^{-6}$
2.2	$2.81\text{x}10^{-6}$
2.6	$3.27\text{x}10^{-6}$
3.0	$3.73\text{x}10^{-6}$

[40%]

2 (a) Draw the circuit diagram of a MOSFET inverting voltage amplifier and explain the Miller effect in such a circuit. [30%]

(b) If an inverting voltage amplifier has a gain A and Miller capacitance C_{GD}, write down the expressions for:

(i) the input current due to the Miller capacitance; [10%]

(ii) the effective input capacitance; [10%]

(iii) the ratio of the amplifier's upper 3dB frequencies with and without the Miller capacitance. [20%]

(c) Discuss why it is important to minimize the Miller effect and how to do so at device level. [30%]

3 (a) The circuit diagram of a FRAM cell is shown in Fig. 1. Please explain how to write and read a bit of information, that is the WRITE and READ operations, in terms of the different voltage levels that are applied to the terminals BL, WL and CP. [Hint: Sense amplifier for read-out is connected to BL.] [50%]

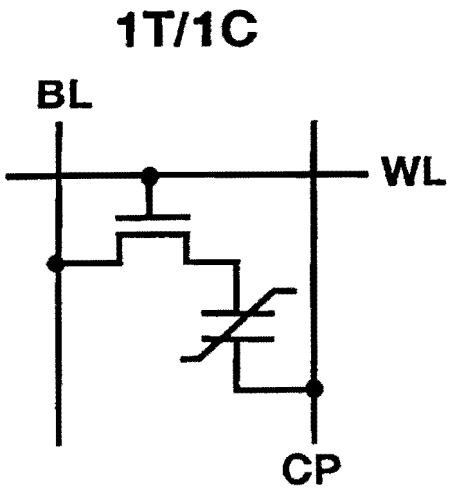

Fig. 1

(b) The ferroelectric capacitor in Fig. 1 is made of a ferroelectric material and its hysteresis curve is shown in Fig. 2. It has dimensions of 100 nm in thickness and $(250\ nm)^2$ in area. Estimate:

(i) the remnant polarisation and coercive field of the material;

(ii) the amount of charge flowing into the bit-line (BL) during a READ operation with a +5 V applied to CP:

(a) when the initial information stored in this memory cell is State "1" (positively polarised);
(b) when the initial information stored in this memory cell is State "0" (negatively polarised).

(iii) the energy consumed by the ferroelectric capacitor due to polarisation switching. [50%]

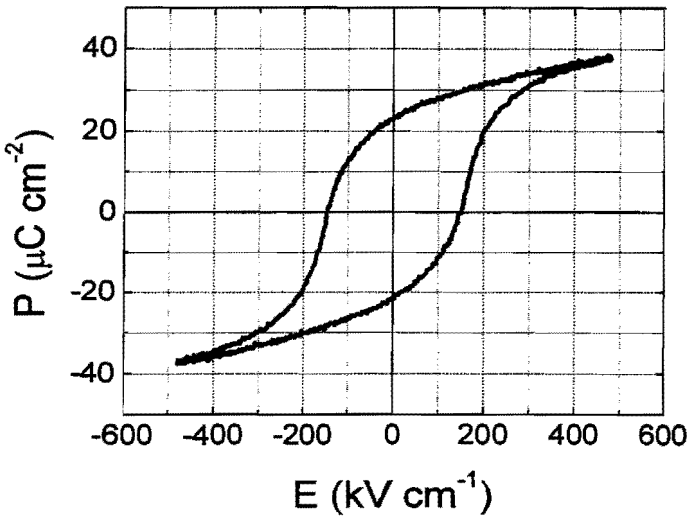

Fig. 2

4 (a) Explain what is the giant magneto-resistance (GMR) effect, including its principle, basic elements and their functions. [30%]

(b) Explain the performance of a GMR unit, based on the experimental results shown in Fig. 3. Explain why $\Delta\rho/\rho$ can be greater than 100%. [40%]

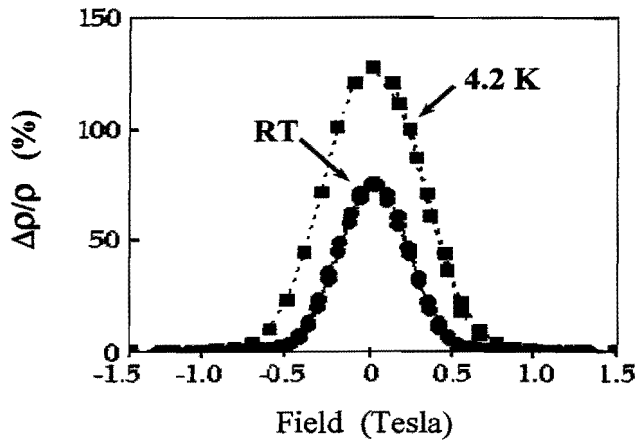

Fig. 3

(c) With reference to Fig. 4, explain the WRITE operation of a pseudo spin valve (PSV) magnetic random access memory (MRAM) array. [30%]

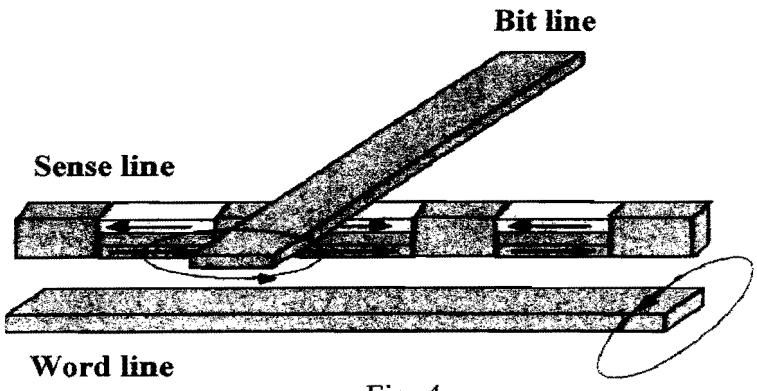

Fig. 4

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