ENGINEERING TRIPOS PART IIB

Tuesday 8 May 2012 9 to 10.30

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

dmh04

1 (a) Describe the main features of a quality assurance system as would be followed in major plants fabricating silicon integrated circuits, covering issues such as customer support, design integrity, quality control in production, and the reliability of the product. [40%]

(b) Describe the bath-tub curve used to characterise failure rates of VLSI products, and give examples of failures that apply in each part of the bath-tub curve. [30%]

(c) Describe the Arrhenius equation as used in reliability modelling, with applications to failures due to the stress of voltage or temperature. [30%]

2 (a) Write extended notes, with annotated diagrams, on the following three improvements that have been made to conventional CMOS technology, describing the reasons why these are improvements and why they have been introduced.

(i) Silicon on insulator technology

(ii) Low k-dielectrics such as hafnium oxide, and

(iii) Multilevel metal interconnections. [60%]

(b) Describe the factors that must be considered when laying out the equipment in a new fabrication facility for VLSI manufacture, and the steps taken to ensure that the equipment is functioning properly. [40%]

3 (a) What is the definition of the *threshold voltage* in a MOSFET? Discuss briefly the major physical and other factors that determine the threshold voltage in a MOSFET. [30%]

(b) The *flash memory* relies for its operation on varying the threshold voltage of a form of MOSFET by electrical means. With the aid of a diagram to show the structure of a flash memory cell, explain how this is accomplished. Hence outline the mode of operation of the flash memory cell, and describe the steps involved in writing data to the device and reading it back. [50%]

(c) What are the main advantages and disadvantages of flash memories compared with other MOS implementations of high density memory? [20%]

4 (a) Describe the circuit structures required in CMOS IC design to convey signals between logic gates comprising small geometry MOSFETs and the output pads. [30%]

(b) Discuss the precautions that are necessary:

(i) to minimise the area occupied by the pad driver;
(ii) to prevent latchup. [10%]

(c) A non-inverting CMOS output pad driver consists of four appropriately designed inverters connected in cascade. It is required to transmit the signal from the output of a minimum geometry inverter to an output pad. The pad itself and the external circuitry connected to it impose a purely capacitive load of 60 pF. The capacitance to substrate measured at the input to the first inverter of the driver is 100 fF, and the channel dimensions W and L of the n-channel transistor used in its construction are 1 μm and 0.5 μm, respectively.

(i) Show how to specify the channel dimensions of the transistors used in the remaining three stages of the pad driver so as to minimise the delay imposed on the transmitted signal, and determine the dimensions and the minimum delay. All stages are to have propagation delays equalised for rising and falling edges. [40%]

(ii) Discuss whether it is possible to devise an alternative design that would be expected to result in a smaller delay, if the driver is still required to provide a non-inverted output. [20%]

You may assume that the delay τ imposed on a signal by a CMOS inverter driving a capacitive load C is given by:

$$\tau = \frac{3C}{\mu C_{OX} V_{DD} (W / L)}$$

where μ is the mobility of the carriers concerned, C_{OX} is the specific capacitance of the gate electrode, V_{DD} is the power supply voltage, and W/L is the channel aspect ratio. Take $\mu_N/\mu_P = 2$, $\mu_N C_{OX} = 2.5 \times 10^{-4}$ AV^{-2}, and $V_{DD} = 3$ V.

5 (a) Explain the meaning of the term *sheet resistance*. Show how this concept can be used during the design of an integrated circuit to predict the resistance of electrical interconnects containing linear elements and a number of right-angle bends. [30%]

(b) Give a simple explanation of the phenomenon of *electromigration* and the factors affecting its appearance. What steps can the integrated circuit designer take to alleviate its effects? [20%]

(c) With a series of annotated diagrams, describe the process steps for the fabrication of an NMOS transistor, including brief notes on each of the processing steps. [30%]

(d) Discuss the factors that must be considered in determining the order in which the various steps in (c) are performed. [20%]

END OF PAPER