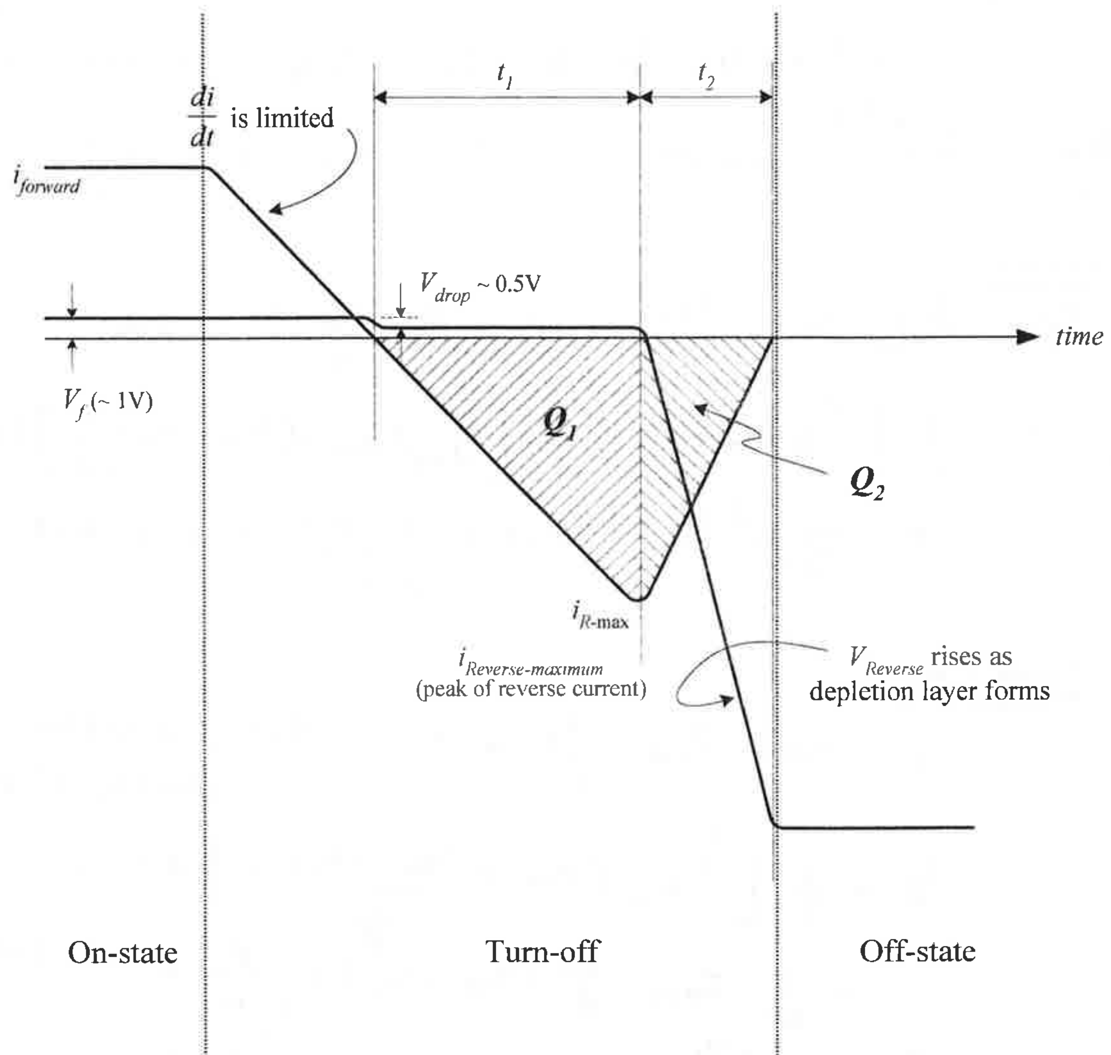
1. (a)




Turn-off

- di/dt is limited by the external circuit. As an attempt is made to reverse-bias the diode, the current starts decreasing and flows in the opposite direction as plasma is still present.
- $Q_1$ is associated with the plasma in the drift region and $t_1$ is the time taken to remove it.
- Once plasma is removed at the end of $t_1$, a depletion region starts to grow and the reverse voltage across the diode can increase. At the end of this region the device can block the voltage and the current decreases to a leakage level.

[30]

(b) The device is an IGBT. The turn-off features a first fall, associated with the drop in the electron current (as the channel (MOS inversion layer) is suppressed) and the second drop is usually associated with the hole sweep out and recombination of plasma. This takes a longer time to remove. $I_h$ is approximately equal to the original hole current at the cathode side (as the electron current drops very fast when the channel is 'killed').

[20]

(b) (ii) $T = \frac{1}{f_s} = \frac{1}{100\,kHz} = 10\,\mu s$ $\quad D = 50\% \Rightarrow DT = 5\,\mu s$

$DT = t_{ON} + t_r + t_d = 5\,\mu s \Rightarrow t_{ON} = 5 - 0.1 - 0.2 = 4.7\,\mu s$

$(1-D)T = t_{off} + t_s + t_g + t_{f1} + t_{f2} \Rightarrow t_{off} = 5 - 0.1 - 0.3 - 0.5 - 0.1 = 4\,\mu s$

STATIC

- **$P_{ON}$** $= \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON}\, dt = V_{ON} \cdot I_{ON} \cdot \frac{t_{ON}}{T} = 3 \cdot 1 \cdot \frac{4.7}{10} = 1.41\,W$

SWITCHING

- **TURN-ON**

$P_r = \frac{1}{T}\int_0^{t_r} V_{DC} \cdot \frac{I_{ON} \cdot t}{t_r} \cdot dt = \frac{V_{DC} \cdot I_{ON} \cdot t_r}{2T} = 2\,W$

- $P_d = \frac{1}{T}\int_0^{t_d} I_{ON} V(t)\, dt = \frac{1}{T}\int_0^{t_d} I_{ON}\left[V_{DC} + (V_{ON} - V_{DC})\frac{t}{t_d}\right] dt =$

$= \frac{I_{ON} \cdot t_d}{2T}(V_{DC} + V_{ON}) = \frac{1 \cdot 0.2}{2 \cdot 10} \cdot 403 = 4.03\,W$

- **TURN-OFF**

$P_s = V_{ON} \cdot I_{ON} \cdot \frac{t_s}{T} = 3 \cdot 1 \cdot \frac{0.1}{10} = 0.03\,W$ (negligible)

$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left[V_{ON} + \frac{V_{DC} - V_{ON}}{t_g} t\right] dt =$

$= \frac{1}{2T} I_{ON} \cdot t_g (V_{ON} + V_{DC}) = \frac{1}{2 \cdot 10} \cdot 1 \cdot 0.3 \cdot 403 = 6.05\,W$

$P_{f1} = \frac{1}{T}\int_0^{t_{f1}} V_{DC}\left[I_{ON} + (I_h - I_{ON})\frac{t}{t_{f1}}\right] dt =$

$= \frac{1}{2T} V_{DC}\, t_{f1}\left[I_{ON} + I_h\right] = \frac{1}{2 \cdot 10} \cdot 400 \cdot 0.1 \cdot 1.3 = 2.6\,W$

$P_{f2} = \frac{1}{T} V_{dc} \cdot t_{f2} \cdot \frac{I_h}{2} = \frac{1}{2 \cdot 10} \cdot 400 \cdot 0.5 \cdot 0.3 = 3\,W$

---

ON-STATE LOSSES = 1.41 W

OFF-STATE LOSSES = 0 W

TURN-ON LOSSES = 2 W + 4.03 W = 6.03 W

TURN-OFF LOSSES = 0.03 + 6.05 + 2.6 + 3 = 11.68 W

TOTAL

TOTAL LOSSES = 1.41 + 6.03 + 11.68 = **19.12 W**

[50%]

2.

(a) **Curvature effect**

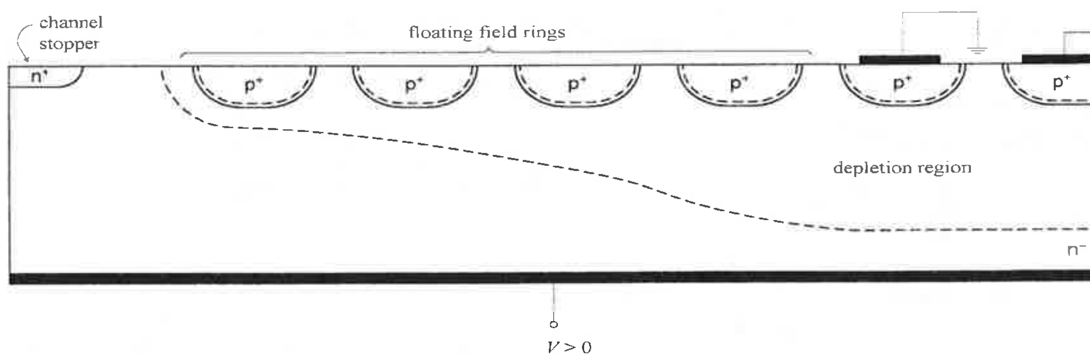
The shape of the junction which supports the voltage plays an important role in 'field crowding'. The higher the radius of a cylindrical or spherical junction the closer the breakdown is to that of an ideal parallel-plane junction. However, in most microelectronics processes the junction depth is limited to a couple of microns up to maximum 10-15 microns. The curvature effect can be reduced in multiple cell power devices such as MOSFETs or IGBTs by placing the cells (with multiple junctions) close together to simulate almost a 'continuous junction'. By solving Poisson's equation for a cylindrical junction one can show that the maximum electric field for the same reverse voltage applied increases significantly compared to that in a planar junction.

**Edge breakdown**

Placing cells very close together has only limited value because at the edge there is always a last cell left 'unprotected'. Premature edge breakdown is a very common effect in power devices. For this, special techniques can be used.

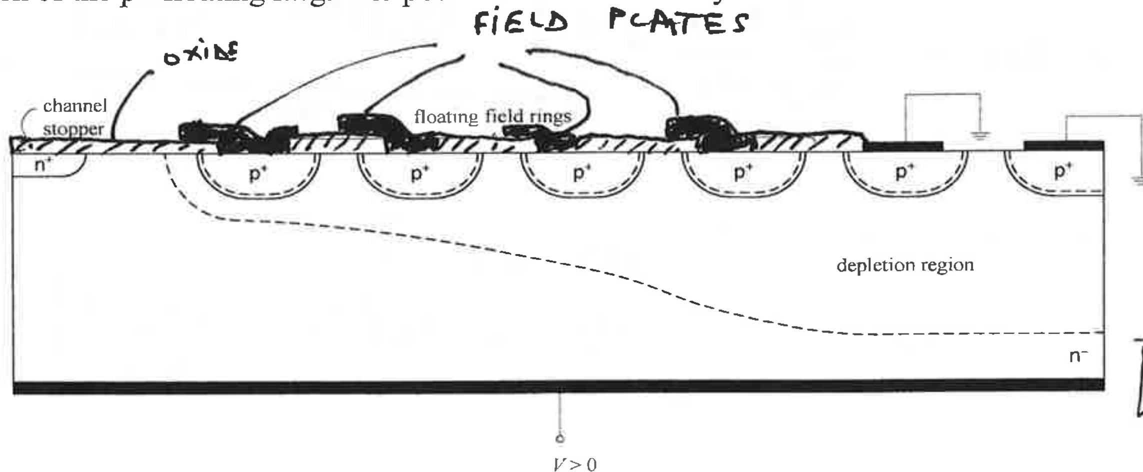
[20%]

A good termination technique is the floating field ring technique. This is based on distributing the field between highly doped p+ floating field rings to alleviate the edge effect.




A similar result can be obtained with the junction termination extension. This is based on having regions of lowly doped p- layers spread out uniformly the electric field at the edge of the device. The p- layers have to be depleted at breakdown.

The field plates placed on each ring help to reduce the electric field at the surface of each of the p+ floating ring. The position is schematically shown below:

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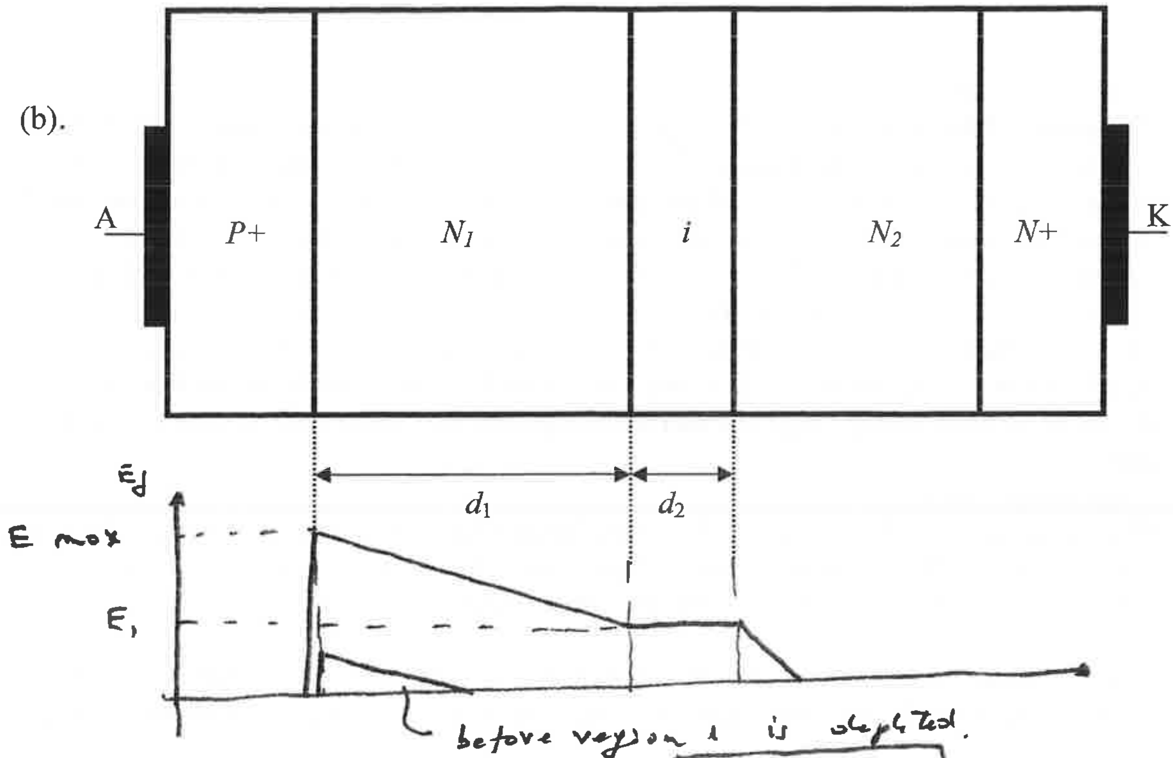



- breakdown occurs when $\boxed{E_{max} = E_{cr}}$

$V_{BR} = V_{PT\ region\ 1} + V_{i\ region\ 2} + V_{NPT\ region\ 3}$

(assuming that region 1 gets depleted before breakdown of the diode)

$$V_{BR} = \frac{1}{2}\left(E_{cr} + E_1\right) d_1 + E_1 d_2 + \frac{\varepsilon_0 \varepsilon_r E_1^2}{2 q N_2}$$

$$E_1 = E_{cr} - \frac{q N_1}{\varepsilon_0 \varepsilon_r} d_1$$

$$\Rightarrow V_{BR} = E_{cr} d_1 - \frac{q N_1}{2 \varepsilon_0 \varepsilon_r} d_1^2 + \left(E_{cr} - \frac{q N_1}{\varepsilon_0 \varepsilon_r} d_1\right)^2 \frac{\varepsilon_0 \varepsilon_r}{2 q N_2} + E_1 d_2$$

$$\Rightarrow V_{BR} = \frac{E_{cr}^2 \varepsilon_0 \varepsilon_r}{2 q N_2} + d_1\left(1 - \frac{N_1}{N_2}\right)\left(E_{cr} - \frac{q N_1 d_1}{2 \varepsilon_0 \varepsilon_r}\right) + E_1 d_2$$

$$\Rightarrow V_{BR} = \underbrace{\frac{E_{cr}^2 \varepsilon_0 \varepsilon_r}{2 q N_2}}_{①} + \underbrace{d_1\left(1 - \frac{N_1}{N_2}\right)\left(E_{cr} - \frac{q N_1 d_1}{2 \varepsilon_0 \varepsilon_r}\right)}_{②} + \underbrace{d_2\left(E_{cr} - \frac{q N_1 d_1}{\varepsilon_0 \varepsilon_r}\right)}_{③}$$

[3-½]

---

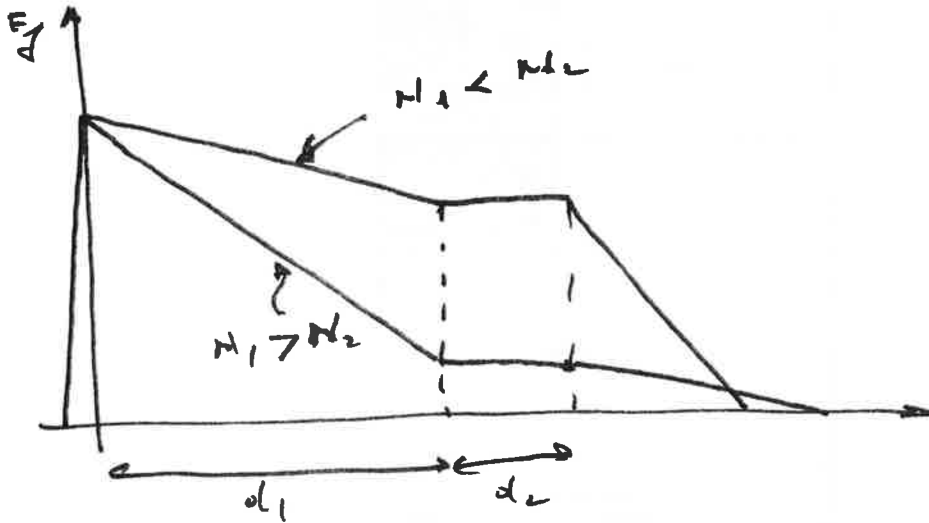
if $N_1 = N_2$ ② $= 0 \Rightarrow$

$$V_{BR} = \frac{E_{cr}^2 \varepsilon_0 \varepsilon_r}{2 q N_1} + d_2\left(E_{cr} - \frac{q N_1 d_1}{\varepsilon_0 \varepsilon_r}\right)$$

if $N_1 > N_2$
② is negative $\Rightarrow$ $V_{BR}$ decreases

if $N_1 < N_2$

(2) is positive $\Rightarrow$ $V_{BR}$ increases

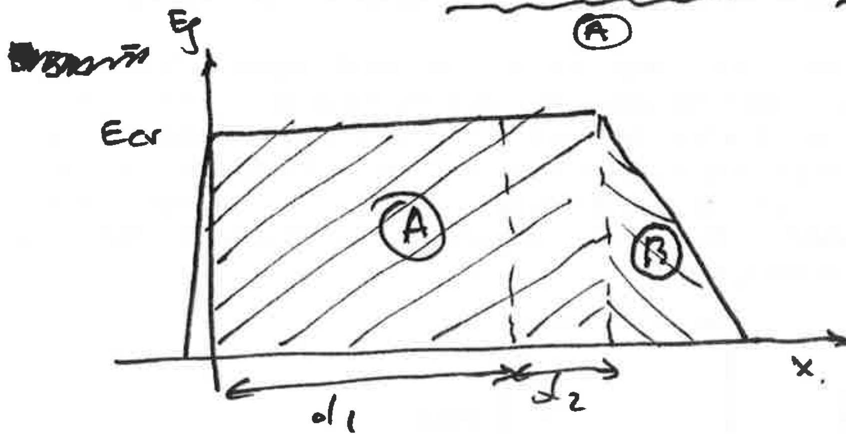



[20%]

(iii) (2) is maximum when $N_1 = 0$
(3) is maximum when $N_1 = 0$

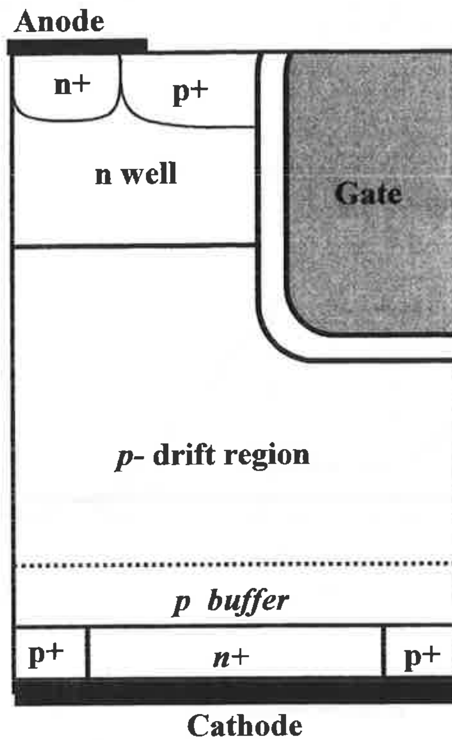
In reality $N_1$ would be equal to $n_i \simeq 10^{10}\ cm^{-3}$ (intrinsic carrier concentration)

for this $V_{BR} = \underbrace{E_{cr}(d_1 + d_2)}_{A} + \underbrace{\frac{E_{cr}^2 \varepsilon_0 \varepsilon_r}{2 q N_2}}_{B}$




[20%]

3. (a)

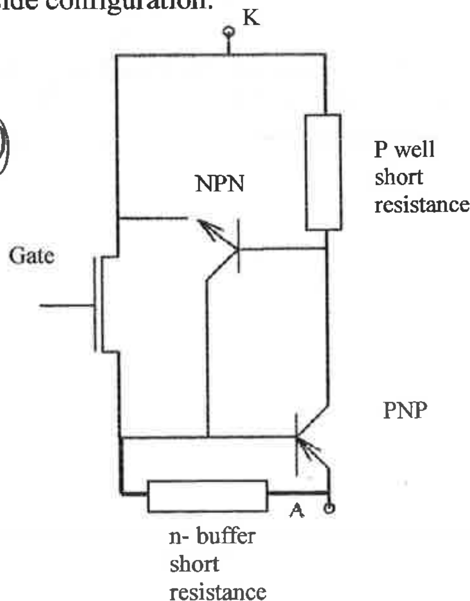



The p+ shorts are connected together with the n+ electron emitter to the cathode terminal. The device could be used in the high side with the anode as high voltage terminal. It features a p-channel and p-drift region. When the gate is negative with respect to the anode and the inversion layer is formed, holes can travel from the p+ anode through the channel to the p-drift region and are collected by the p+ shorts. Once the n+/p buffer junction becomes forward biased, electrons are injected from the n+ emitter into the p-drift region and via the action of the npn transistor as well as that of the PIN diode, conductivity modulation (formation of plasma) takes place in the p-drift region resulting in low on-state resistance. The turn-off process is fast, as the npn transistor is weak (due the shorts) resulting in less plasma and additionally the shorts can collect holes during the turn-off process.

- Compared to a p-channel IGBT, the cathode-shorted p channel IGBT features a snap-back (due to the transition from a unipolar device to a bipolar device). However it is expected to be faster with lower turn-off losses (see above for the reason).
- Compared to an anode-shorted n-channel IGBT, the cathode-shorted p channel IGBT has higher on-state losses due to higher channel resistance. The n-channel would operate in the low-side configuration while the p-channel would operate in the high side configuration.

[30%]

(b)

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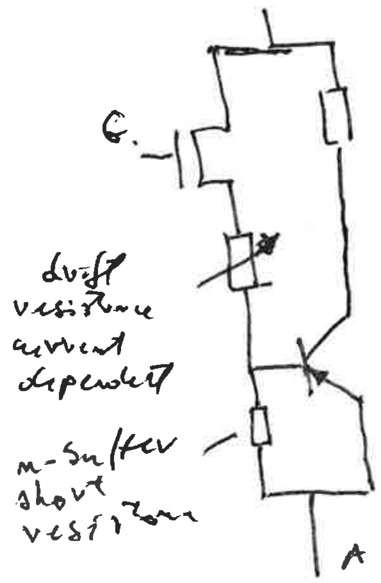
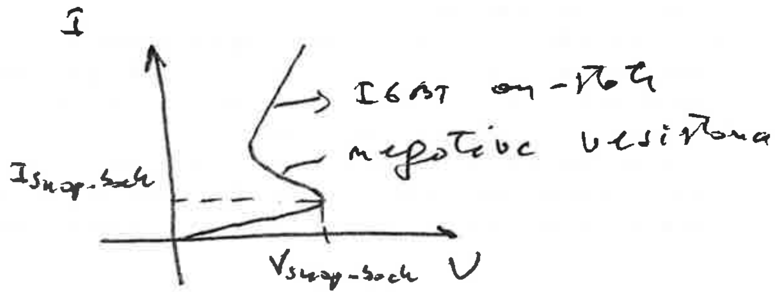
(ii)




~~(ii)~~ Initially the current is formed of electrons only and flows solely through the channel (drift region and the n-buffer short resistance (before the snap-back). The bipolar conduction occurs only when the anode junction becomes forward-biased.

$$I_{snap-back} \cdot R_s = 0.7V$$

$$\Rightarrow I_{snap-back} = \frac{0.7}{10} = 70\ mA$$

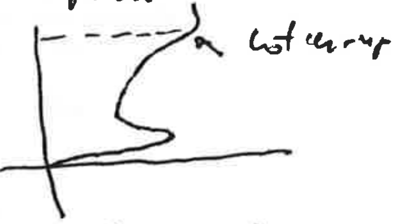
$$V_{snap-back} = (\underbrace{R_{ch} + R_{acc}}_{50\,\Omega} + \underbrace{R_{drift} + R_{spr}}_{20\,\Omega}) I_{snap-back} + 0.7V =$$

$$= 70 \cdot 0.07 + 0.7 = 5.6\ V$$

* The voltage drop on the channel at the snap-back current (70 mA) is 1.4 V ≪ $V_G - V_T = 10V$ which justifies that the MOS is in the linear region [30%]

(iii) Latch-up will occur when drop $I_A \cdot R_{pwell} = 0.7V$

$$\Rightarrow I_A = \frac{0.7}{0.3 \cdot 1} = 2.33\ A$$

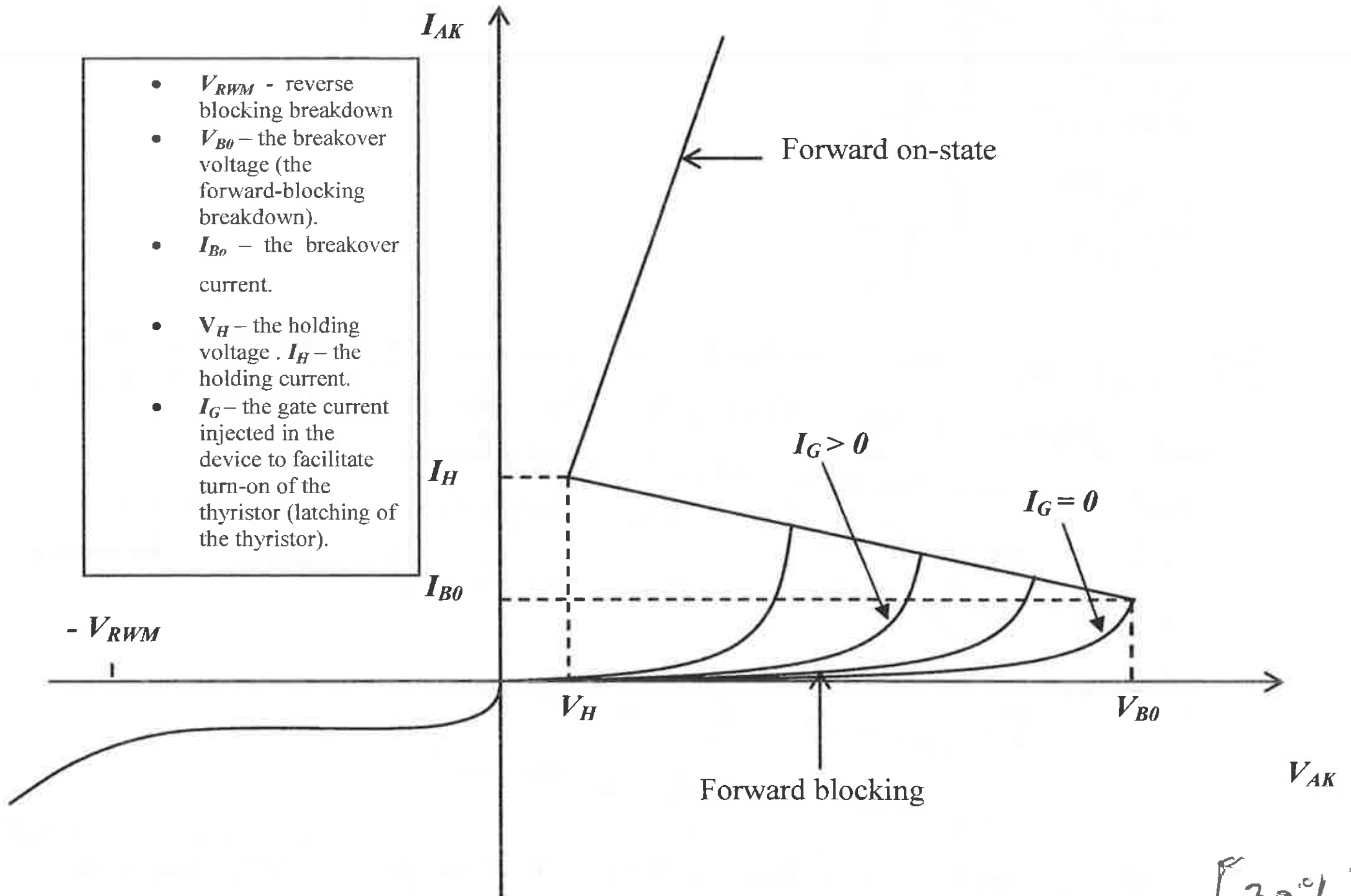



If the Temperature is raised then the voltage drop on the $n^+$/pwell diode will drop with 2mV/°C ⇒ 0.1V

$$\Rightarrow I_A = \frac{0.6}{0.3 \cdot 1} = 2\ A$$

~~[20%]~~ [20%]

4 (a) **Symmetrical thyristors (NPT)** have both forward and reverse blocking capability. In the forward blocking state the anode is biased positive with respect to the cathode, while in the reverse blocking state the anode is biased negative with respect to the cathode. Symmetrical thyristors are based on a NPT junction design. The device has however reverse-blocking capability which can be of use in special power electronic circuits. In addition, these devices can be turned-off by reverse biasing the voltage between anode and cathode.
**Aymmetrical thyristors (PT)** have only forward blocking capability. They are based on a PT junction design and they feature a buffer between the n- drift region and the p-anode to make sure that no punch-through breakdown occurs. The lowly doped drift region is however fully depleted at breakdown. When compared to the symmetrical thrristors, the asymmetrical thyristors have thinner n- drift region and therefore reduced on-state and transient losses. Because they do not offer reverse blocking capability, they cannot be turned-off by reversing the anode-cathode voltage. For this reason most of the asymmetrical thyristors are GTOs or GCTs where the turn-off is accomplished via the gate.




[30%]

(b) This effect is very severe during turn-off when a high forward voltage is re-applied to the structure. There is a maximum $dV/dt$ rating above which the displacement current created through the junction capacitance will be greater than the breakover current, thus resulting in a parasitic re-turn-on (the device refuses to turn-off).

One solution to minimize the effect of the $dV/dt$ (in other words, to increase the maximum $dV/dt$ rating). The shorts can collect some of the displacement current which could otherwise turn-on the npn transistor. Since a large component of the displacement current is safely absorbed via the cathode shorts, the slope $dV_F/dt$ can be higher without triggering the parasitic re-turn-on of the thyristor. The smaller the short resistance $R_s$, the more effective the cathode short is, and the higher the maximum $dV_F/dt$ rating.
There are two more advantages resulting from the use of cathode shorts:

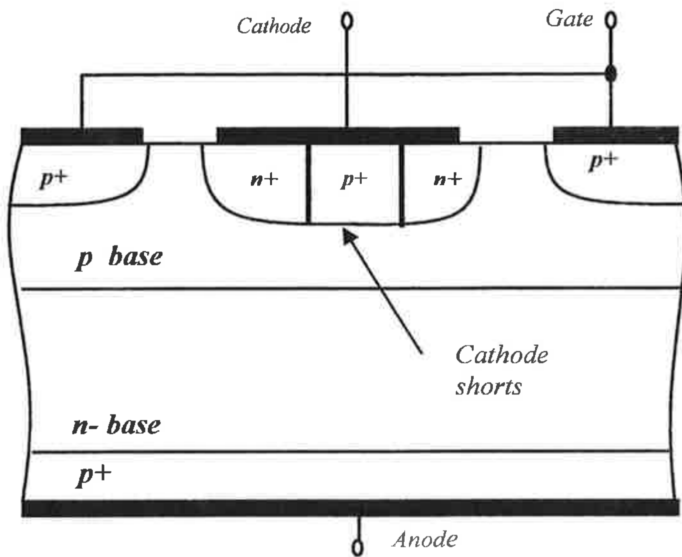
(i) the increase in the breakover point – this gets closer to the maximum breakdown (dictated by avalanche)

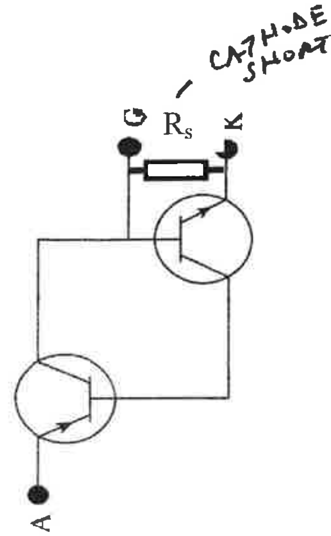
(ii) a faster turn-off. This is due to lower plasma injection

There are however two major drawbacks:

(iii) the turn-on is slightly slower (as the npn transistor is weakened by the shorts).

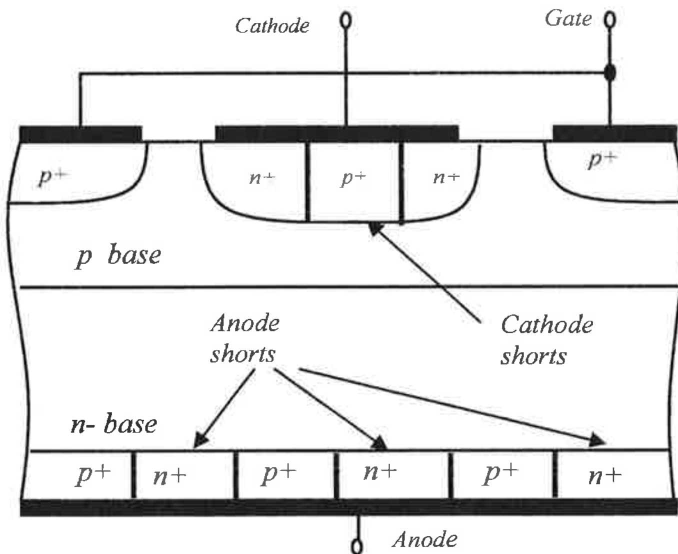
(iv) The on-state losses are slightly higher as the npn transistor has lower gain and therefore the plasma injection will be slightly weaker.

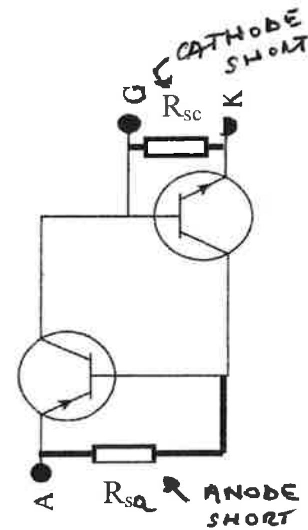



[30%]

(c) ~~(b)~~




The shorts would lower the gain of the pnp and npn transistors resulting in less plasma formation. The turn-off losses would be lower, but the device will be more difficult to turn-on. The presence of the anode shorts and cathode shorts leads to the formation of an anti-parallel diode (p+ shorts & pbase/n-base & n+). This diode prevents a reverse blocking voltage to be applied. Therefore the device cannot turn-off in a similar manner to a classical thryristor by applying a high reverse voltage between anode and cathode. The device can only operate as a GTO (or GCT) with the gate used for both the turn-on process (positive current pulse) and turn-off process (negative current pulse). The equivalent circuit would be that of a GTO with an anti-parallel PIN diode.

[40%]

Note: The device could also experience problems at startup when the potentials on the anode and cathode are zero and the gate is biased. There is a parasitic PiN diode between the gate and the anode which becomes forward-biased.