ENGINEERING TRIPOS   PART IIB

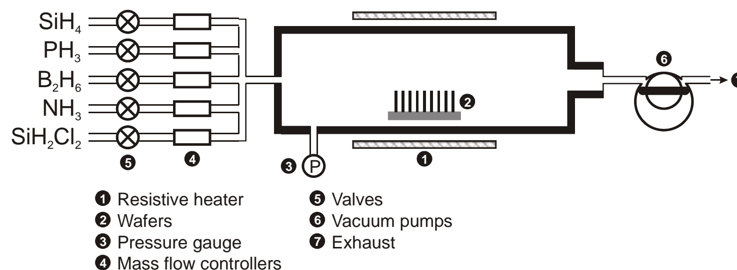
Monday 29 April 2013   2 to 3.30

Module 4M6 - ANSWERS

ajf02

1 (a) This device requires a layer of silicon which is removed from the substrate. This implies that the layer has been controllably released from the substrate, which requires the use of an underlying sacrificial material. Therefore, the layer of silicon cannot be epitaxially grown on the silicon substrate, but must be formed independently on top of the sacrificial material. Crystalline silicon is therefore not a viable option. Silicon is a good MEMS material due to its low density and high Young modulus, and there are highly selective etches for silicon dioxide and silicon. Therefore, it would be preferential if the later were still silicon-based. Amorphous silicon and polycrystalline silicon can both be produced in thin films. However, as we will be depositing onto silicon dioxide and silicon, there are no major thermal constraints, and so polycrystalline silicon would be preferred due to its improved mechanical properties over amorphous silicon, despite the higher deposition temperature.

(b) Very high quality poly-Si can be produced by LPCVD (see Lecture 4) using 100% SiH_4 at a pressure of ~100 Pa, which is fed into a chamber as shown in the figure:



The substrates, which are stacked vertically, are heated at ~600 °C, which is sufficient to thermally induce a chemical reaction on the surface of the substrate forming polycrystalline silicon by

$$SiH_4 \rightarrow Si + 2H_2$$

The material may be readily doped by introducing a dopant containing gas during deposition (or alternatively diffusion or implantation may be used post-deposition).

An alternative to direct deposition of poly-Si layers is the crystallisation of a-Si:H films. a-Si:H can be deposited at below 300 °C either by rf-PECVD or sputtering in a thin film. The film can then be crystallised by heating the material. There are two basic methods for achieving this crystallisation.

The simplest method is to anneal the sample in an inert atmosphere in a furnace. Growth is a two stage process. Initially, small crystalline regions are nucleated in a process which is driven by the fact that the crystalline phase represents a lower Gibbs Free Energy than the amorphous phase. This energy gain is counterbalanced by the surface energy required to maintain the boundary between the two phases. Therefore, crystals below a certain size (the critical cluster size) are energetically unfavourable, as they have a large surface to volume ratio. Once a crystal has nucleated, it grows. Using this technique, full crystallisation can be completed in a few hours at temperatures ~650 °C.

An alternative to thermal annealing is excimer laser annealing. In this technique, an excimer (excited dimer) laser, operating at UV wavelengths, is used to provide a short pulse of photons to a small area of a-Si which has first been dehydrogenated by heating to 450 °C for several hours. The laser light is all absorbed by the a-Si:H layer which is locally heated to aver 1000 °C, inducing a localised crystallisation. By scanning the laser

beam over the material surface between pulses, a larger area may be successfully crystallised. The substrate, however, remains cool as all of the energy remains in the silicon layer, permitting use of this process even on plastic substrates. However, because only a very small region is crystallised in one shot, this process is very slow.

(c) The process flow is as follows:

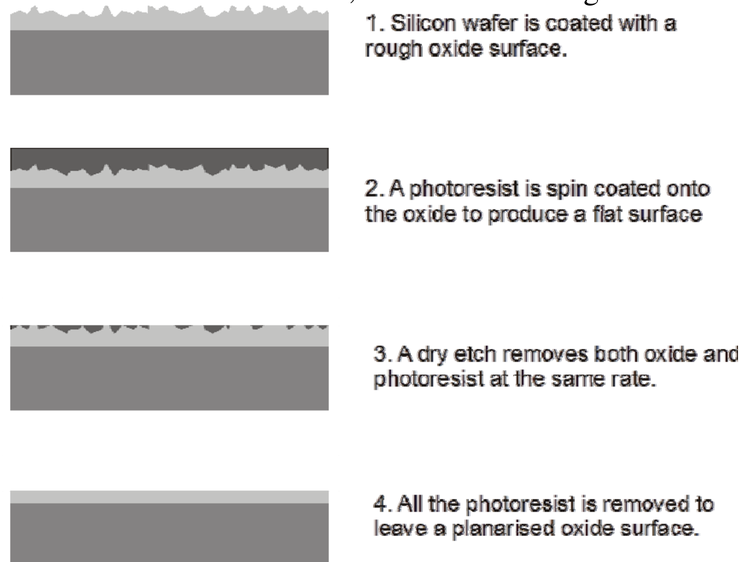
Step	*Code*	*Description*
1	RCA1	Boil a 4" silicon (100) wafer in RCA Clean 1 ($NH_3(aq):H_2O:H_2O_2$) to remove organic contaminants.
2	RCA2	Boil the silicon substrate in RCA Clean 2 ($HCl:H_2O:H_2O_2$) to remove metallic ion contaminants.
3	OXI1	Form a 5 μm thick layer of silicon dioxide on both sides of the wafer by wet thermal oxidation at ~1250 °C
4	PHO1	Spin a layer of photoresist onto the bottom side of the silicon wafer.
5	BAK1	Pre-bake the photoresist.
6	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist which will form a series of holes which will later be removed by DRIE.
7	DEV1	Develop the photoresist.
8	BAK2	Post-bake the photoresist to harden it.
9	RIE1	Use a CF_4 plasma to etch the silicon dioxide exposed through the photoresist on the backside of the wafer.
10	DIW1	Rinse in DI water and blow dry.
11	PHO2	Spin a layer of photoresist onto the top side of the silicon wafer.
12	BAK3	Pre-bake the photoresist.
13	EXP2	Expose the photoresist through a mask to produce a pattern in the photoresist which protect the silicon dioxide where we want the polysilicon to be released from the substrate..
14	DEV2	Develop the photoresist.
15	BAK4	Post-bake the photoresist to harden it.
16	RIE2	Use a CF_4 plasma to etch the silicon dioxide exposed through the photoresist on the top of the wafer.
17	DIW2	Rinse in DI water and blow dry.
18	LPC1	Deposit a 1 μm thick layer of polycrystalline silicon by LPCVD over the top side of the wafer.
19	PHO3	Spin a layer of photoresist onto the top side of the silicon wafer.

20	BAK5	Pre-bake the photoresist.
21	EXP3	Expose the photoresist through a mask to produce a pattern in the photoresist which protect the polycrystalline silicon where we wish to form the membranes and supports.
22	DEV3	Develop the photoresist.
23	BAK6	Post-bake the photoresist to harden it.
24	RIE3	Use a CF_4+O_2 plasma to etch the polycrystalline silicon exposed through the photoresist on the top of the wafer.
25	DRI1	Deep reactive ion etch the back side of the wafer to remove the silicon beneath the polysilicon membranes to stop on the silicon dioxide.
26	BHF1	Use a buffered HF acid etch to remove all silicon dioxide to leave the finished structure.
27	DIW3	Rinse in DI water and blow dry.

2 (a) The surface topography of a sample may be determined using profilometry. A sharp tip (usually ~10 μm radius) is pressed onto the sample surface with a known force (~ 1 mg) and scanned over the surface. The vertical deflection of the tip is measured to give a plot of the topography. This is data may then be used to determine the surface roughness.

(b) The surface could be planarised by chemical mechanical polishing (CMP). A rotating platen is pressed against the surface to be planarised and a slurry injected betwem the two surfaces. The slurry contains both an abrasive and a chemical etchant, and the two actin tandem to produce a faster etching rate than either can achieve alone (faster even than the algebraic sum of the two etch rates) to yield a very flat surface. CMP does have its disadvantages. It uses very large quantities of slurry. There is an etch rate dependency on pattern density and material type. Dummy structures are frequently required to ensure a uniform etch over a whole surface.

Therefore, an alternative would be to use resist etchback. The rough zinc oxide surface is coated in a polymer which has similar dry etch characteristics to the oxide. The polymer will tend to form a smooth surface due to surface tension. After drying and curing, the polymer coated oxide is dry etched. This transfers the smooth topography of the polymer surface back to the oxide surface, as shown in the figure:



The disadvantage of this technique is that it requires a polymer to be found with the same etch characteristics as the zinc oxide, which is not trivial.

(c) Ellipsometry could be used to determine the thickness of eth zinc oxide film after planarisation. Without any step edges, profilometry would not be appropriate, whilst the optical transparency of the zinc oxide means that the laser light from the ellipsometer would easily penetrate the film. Also, as it is smooth, the ellipsometer would be able to give an accurate reading as it samples over a significant area.

(d) Photolithography resolution is determined by the film thickness according to

$$R = \frac{3}{2}\sqrt{\lambda\left(s + \frac{z}{2}\right)}$$

where R is the resolution, λ is the wavelength of light, s is the print gap and z is the film thickness. A large surface roughness will mean that resolution is compromised by the variable thickness of the photoresist. There is also an increase likelihood of light scattering from the rough surface, which compromises resolution. It is also likely that photoresist in 'trenches' caused by the large roughness will not be properly exposed whilst photoresist on 'hills' will be overexposed. The result will be very poor pattern transfer.

3 (a) Resists are broadly classified into two categories:

Positive tone resists

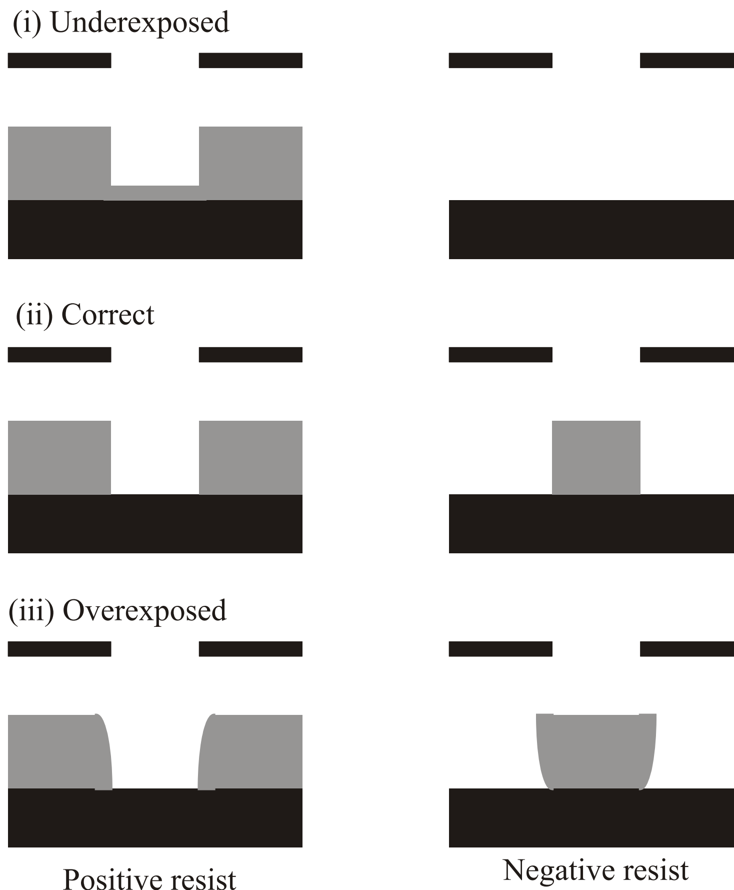
Exposure of the resist to high energy photons in the deep UV causes scission of the polymers chains. The weakened polymer may then be removed by a developer solution (usually a weak base, such as KOH) in the exposed region. Positive resists may be completely stripped by strong bases.

Negative tone resists

Exposure of the resist either causes cross-linking of the polymer chains to create large molecular weight chains which are insoluble, or induce a photochemical change to an insoluble polymer. Water based developers are most frequently used, but a few organic based developers do still remain.

There are a number of factors which might affect the choice of photoresist. Positive resists give higher resolution, and so are preferred if small features are to be created. Positive resists are also less sensitive to pinhole formation, leading to a better yield. Negative resists, however, have a better resistance to wet and dry etching and so make better etch masks. They can also be developed to produce overhanging edges which is preferred for lift-off patterning.

(b)



(c) (i) Resolution is given (from the Data Book) by

$$R = \frac{3}{2}\sqrt{\lambda\left(s + \frac{z}{2}\right)}$$

Therefore, for the SU8:

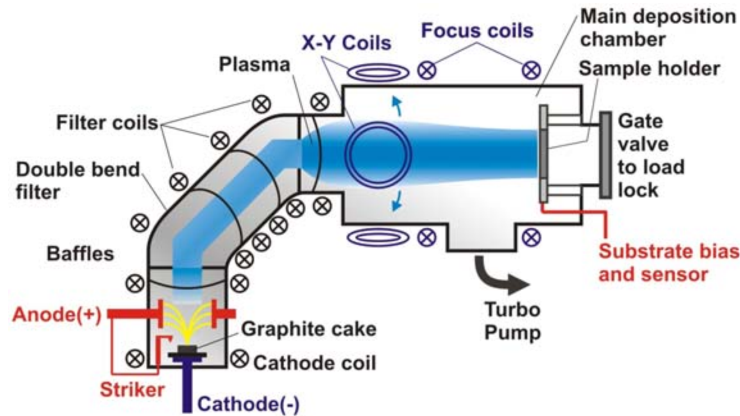
$$R = \frac{3}{2}\sqrt{190\times10^{-9}\left(5\times10^{-6} + \frac{10\times10^{-6}}{2}\right)} = 2.1\ \mu\text{m}$$

For the AZ5214E:

$$R = \frac{3}{2}\sqrt{190\times10^{-9}\left(5\times10^{-6} + \frac{2\times10^{-6}}{2}\right)} = 1.6\ \mu\text{m}$$

(ii) Due to the finite resolution of the SU8, the actual lateral sides of the well could be as large as 10 µm+(2×2.1 µm), giving 14.2 µm. In addition, the silicon nitride could be smaller than x by 2×1.6 µm, which is 3.2 µm. This would suggest a minimum value of x of 14.2 µm+3.2 µm, giving 17.4 µm. However, there is also the possibility of the SU8 being misaligned by 1 µm to either side, so we should add 2 µm to the dimension x. Hence, the actual minimum size of x is 19.4 µm.

4 (a) A schematic diagram of the filtered cathodic vacuum arc (FCVA) is shown in the figure:



The source of carbon in the FCVA is a block of graphite that sits inside a vacuum. A high current is passed through the graphite block using a graphite pin at a local point (~80 A) which causes a graphite to heat up and sublime. Carbon is emitted from the surface of the graphite in many forms from individual C^+ ions (and electrons) to large carbon macroparticles. This conductive plasma arc makes an electrical connection to the chamber wall, allowing the pin to be removed. A current coil produces a magnetic field which sweeps the emitted electrons round an s-shaped bend. The electric field produced is sufficiently strong for C^+ ions to be pulled round the bend, whilst larger particles are 'lost' to the chamber walls. In this way, a beam of only C^+ ions is generated.

The key parameter for ensuring that the material is diamond-like is the energy of the C^+ ions. Ions with ~100 eV kinetic energy hit the growing ta-C surface and have sufficient energy to subplant themselves a few atomic layers below the surface. Their kinetic energy is converted to thermal energy as they slow down. This thermal energy induces a phase transition to the sp^3 state, resulting in material which is ~80% sp^3 bonded. If the ion energy is much lower than 100 eV then subplantation does not occur and a polymeric film results, whilst if the ion energy is too high, then the sample is able to relax back to the graphitic state.

This subplantation process leads to high compressive stress, and so thick films tend to delaminate from the substrate.

(b) (i) The process flow is as follows:

1	RCA1	Boil a 4" silicon (100) wafer in RCA Clean 1 (NH_3(aq):H_2O:H_2O_2) to remove organic contaminants.
2	RCA2	Boil the silicon substrate in RCA Clean 2 (HCl:H_2O:H_2O_2) to remove metallic ion contaminants.
3	FCV1	Deposit a 20 nm thick layer of tetrahedral amorphous carbon over the silicon wafer.

4	SPU1	Rf magnetron sputter deposit a 5 μm thick layer of silicon dioxide on top of the tetrahedral amorphous carbon from a silicon dioxide target.
5	SPU2	Magnetron sputter deposit a 2 μm thick layer of tungsten on top of the silicon dioxide.
6	PHO1	Spin a layer of photoresist onto the top side of the silicon wafer.
7	BAK1	Pre-bake the photoresist.
8	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist which will protect the tungsten cantilevers.
9	DEV1	Develop the photoresist.
10	BAK2	Post-bake the photoresist to harden it.
11	PER1	Use a 30% H_2O_2 wet etch to etch the exposed tungsten. This will automatically stop on the silicon dioxide.
12	DIW1	Rinse in DI water and blow dry.
13	BHF1	Etch the silicon dioxide with buffered hydrofluoric acid. This will not affect the silicon substrate, the tetrahedral amorphous carbon or the tungsten. However, it should be timed so that the etch is stopped as soon as the cantilevers are undercut.
14	DIW2	Rinse in DI water.
15	IPA1	Rinse in isopropanol.
16	ACE1	Ultrasonicate in acetone to remove any residual photoresist.
17	ACE2	Rinse in fresh acetone and gently blow dry to avoid stiction.

(c) Tetrahedral amorphous carbon has a very low surface energy, and so coating the silicon in it will reduce the likelihood of the tungsten cantilever from permanently adhering to the substrate during operation (which is likely as this is the purpose of the switch). An alternative would be to use a self-assembled monolayer (SAM) (such as octadecyltrichlorosilane) which also has a very low surface energy. However, SAMs lack the mechanical robustness of carbon.