ENGINEERING TRIPOS PART IIB

Tuesday 30 April 2013 14:00 to 15.30

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

F. UDREA
17 MAY 2013

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. Fig. 1 shows a simplified inductive switching circuit for a high voltage system such as a Switch Mode Power Supply (SMPS).

(a) Assuming that the switch S is ideal, draw the current and voltage waveforms of the silicon PIN diode, D_f, as a function of time, during on-state, turn-off and off-state. Explain the significance of the distinctive time intervals during the turn-off. [30%]

(b) Assume now that the switch is not ideal and its waveforms are as shown in Fig. 2. The switch operates at a switching frequency of 100 kHz with a duty cycle D = 50%. The other circuit parameters are: the gate voltage $V_{G\text{-}on}$ = 15 V, the rail voltage V_{dc} = 400 V, the off-state leakage current I_{OFF} can be neglected (I_{OFF} =0), the on-state current I_{ON} = 1 A, the on-state voltage V_{ON} = 3 V, the turn-on delay time t_d = 0.1 μs, the rise time t_r = 0.2 μs, the turn-off delay time t_s = 0.1 μs, the turn-off voltage growth time t_g = 0.3 μs, the fast current fall time t_{f1} = 0.1 μs, and the slow current fall time t_{f2} = 0.5 μs. Assume the current at the end of the fast current fall is I_h = 0.3 A.

(i) What device is likely to have the waveforms shown in Fig. 2? Justify your choice. What is the significance of the current I_h? [20%]

(ii) Estimate the static, switching and total power losses in the switch. [50%]

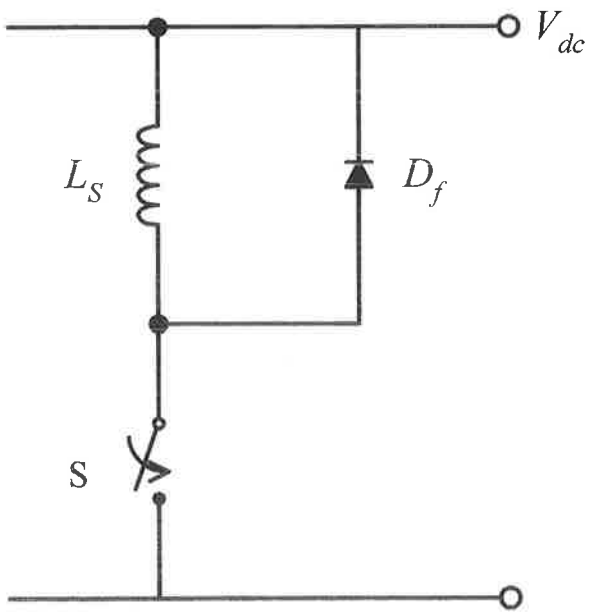

Fig. 1

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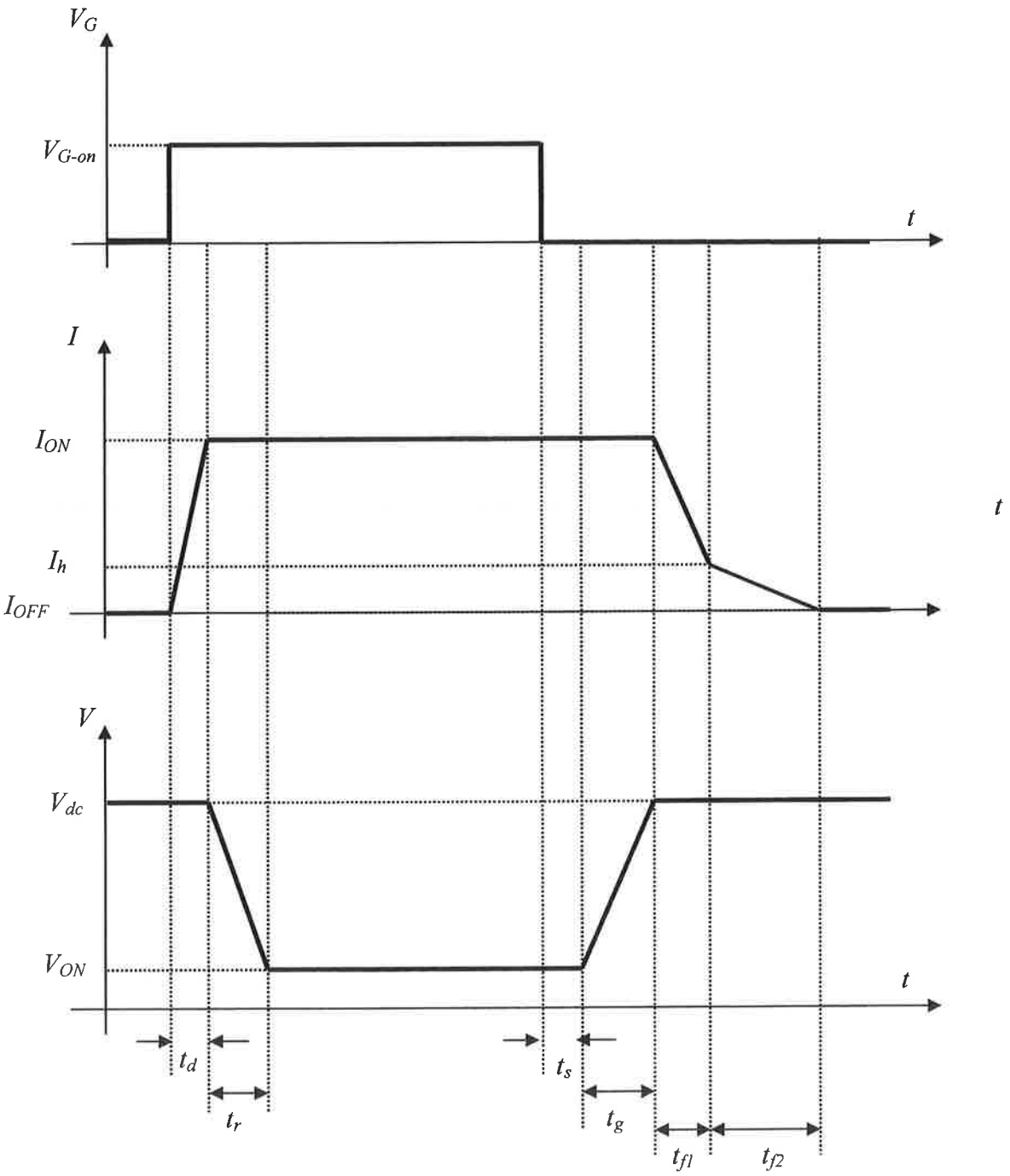

Fig. 2

(TURN OVER

2. (a) Explain the edge and curvature effects in high voltage devices and briefly describe one termination technique to reduce these effects. [20%]

Explain why a field ring termination design is usually used together with the field plate design. Show the position of the field plates on each of the field rings. [10%]

(b) The Non-Punch-Through (NPT) power diode shown in Fig. 3 has the drift region split into three regions with different doping concentrations N_1, i and N_2 where i is an intrinsic region. The width of the first region is d_1 and the width of the second region is d_2. Assume that the third region with doping concentration N_2 is sufficiently long so that the diode remains in non-punch-through state at breakdown.

(i) Sketch the electric field distribution as a function of the distance across the diode, and calculate the breakdown voltage as a function of the doping concentrations N_1 and N_2, the widths d_1 and d_2 and the critical electric field in the semiconductor. [30%]

(ii) Analyse the expression of the breakdown voltage and sketch a graph of the electric field as a function of distance if $N_1 = N_2$, $N_1 > N_2$ and $N_1 < N_2$. [20%]

(iii) If N_2, d_1 and d_2 are fixed, find the optimal doping concentration N_1 to yield maximum breakdown voltage. [20%]

You may assume the following equation in an abrupt one-dimensional p+/n- junction:

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

where w is the depletion region width, N_D is the doping concentration of the n- side of the junction, V is the reverse voltage and the other symbols have their usual meaning.

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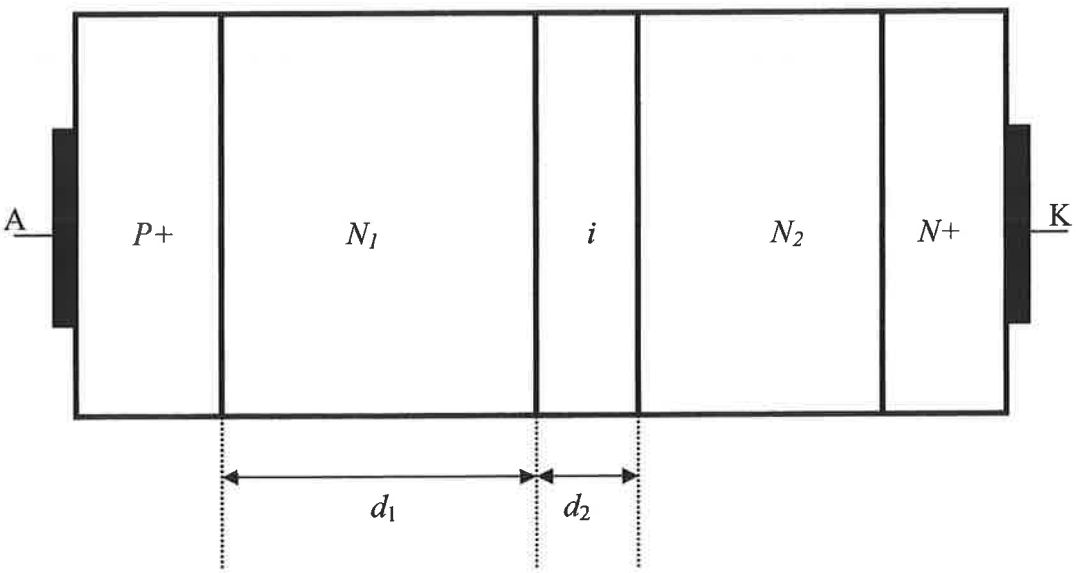

Fig. 3

3. (a) Draw schematically the cross-section of a cathode-shorted p-channel vertical trench IGBT structure. Describe the operation of the device highlighting the main advantages and disadvantages of this structure compared to both a p-channel vertical trench IGBT and an anode-shorted n-channel vertical trench IGBT. [30%]

(b) An anode-shorted, n-channel vertical trench IGBT has an equivalent n-buffer short resistance (i.e. the resistance that appears in parallel with the base-emitter junction of the pnp transistor) of 10 Ω. The doping resistance of the drift layer, which includes the spreading resistance from the accumulation layer, is 50 Ω. The channel resistance, which includes the accumulation layer resistance, is 20 Ω. The gate voltage with respect to the cathode V_G = 15 V and the threshold voltage V_T = 5 V. The equivalent short resistance of the p-well (i.e. the resistance that appears in parallel with the base-emitter junction of the parasitic npn transistor) is 1 Ω. The effective current gain α_{pnp} when the device is in the normal operating on-state condition is 0.3.

(i) Draw the equivalent circuit of the device, including the parasitic npn transistor, the n-buffer short resistance and the p-well short resistance. [20%]

(ii) Find the snap-back voltage and current, where the device changes from a unipolar mode into a bipolar mode. State any assumptions made. [30%]

(iii) Find the latch-up current. Explain what would happen if the device temperature were to be raised by 50°C due to self-heating. State any assumptions made. [20%]

4. (a) Highlight the differences between a symmetrical and an asymmetrical thyristor. Draw schematically the static I-V characteristics of a symmetrical thyristor and describe the main regions/parameters associated with them. [30%]

(b) Explain the *dV/dt* effect in thyristors and state the condition for the parasitic re-triggering of the thyristor during turn-off. Propose one solution to minimise the *dV/dt* effect and discuss the main advantages and disadvantages (if any) of this solution. [30%]

(c) Draw the cross-section and the equivalent circuit of a double shorted (both anode-shorted and cathode-shorted) thyristor. Describe its operation in the major modes of operation with particular emphasis on the turn-off process. Comment on the performance of the double shorted thyristor compared to those of classical and GTO thyristors. [40%]

END OF PAPER

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4B2 Numerical Solutions

Q1: On-state losses: 1.41W
Off-state losses: ~0W
Turn-on Losses: 6.03W
Turn-off Loses: 11.68W
Total Losses: 19.12W

Q3 (b) (ii) $I_{snap\text{-}back}$ =70mA (considering a forward-voltage of the junction as 0.7V)
$V_{snap\text{-}back}$ =5,6V

(iii) $I_{Alatch\text{-}up}$=2.33A
When the temperature is raised by 50C, $I_{Alatch\text{-}up}$=2A