ENGINEERING TRIPOS   PART IIB

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Tuesday 23 April 2013   9.30 to 11.00

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Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

STATIONERY REQUIREMENTS   SPECIAL REQUIREMENTS
Single-sided script paper   Engineering Data Book
                                       CUED approved calculator allowed
                                       Supplementary pages:
                                       One extra copy of Fig. 1
                                       (Question 1).
                                       One extra copy of Fig. 2
                                       (Question 2).

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

dmh05

1   (a)   Describe the use of copper metallisation and double polysilicon in VLSI technologies.   [20%]

(b)   Fig. 1 is a plan layout of a CMOS technology gate, where A is the 3V power supply rail and B is the ground line.

(i)   Explain the logic function of the device and the functions of the connections C, D, E, F and G.   [10%]

(ii)   Identify on the answer sheet copy of Fig. 1 which transistors are p-type and which are n-type.   [10%]

(iii) A major error has been made in the layout shown in Fig. 1. Identify and explain this error and, on the answer sheet copy of Fig. 1, redraw the layout to eliminate this error.   [10%]

(iv) Estimate the approximate linewidth of the CMOS process.   [10%]

(v)   Sketch on the answer sheet copy of Fig. 1 a suitable location for an n-type well in the p-type silicon substrate. Label the regions which are implanted with n-type dopants, and explain the electrical function of the structure near the point X=19, Y=6 in Fig. 1.   [20%]

(vi) Draw a cross-section through the transistor structures along the line Y=11 from X=0 to X=19 and identify the various conducting layers and their electrical function in the device.   [20%]
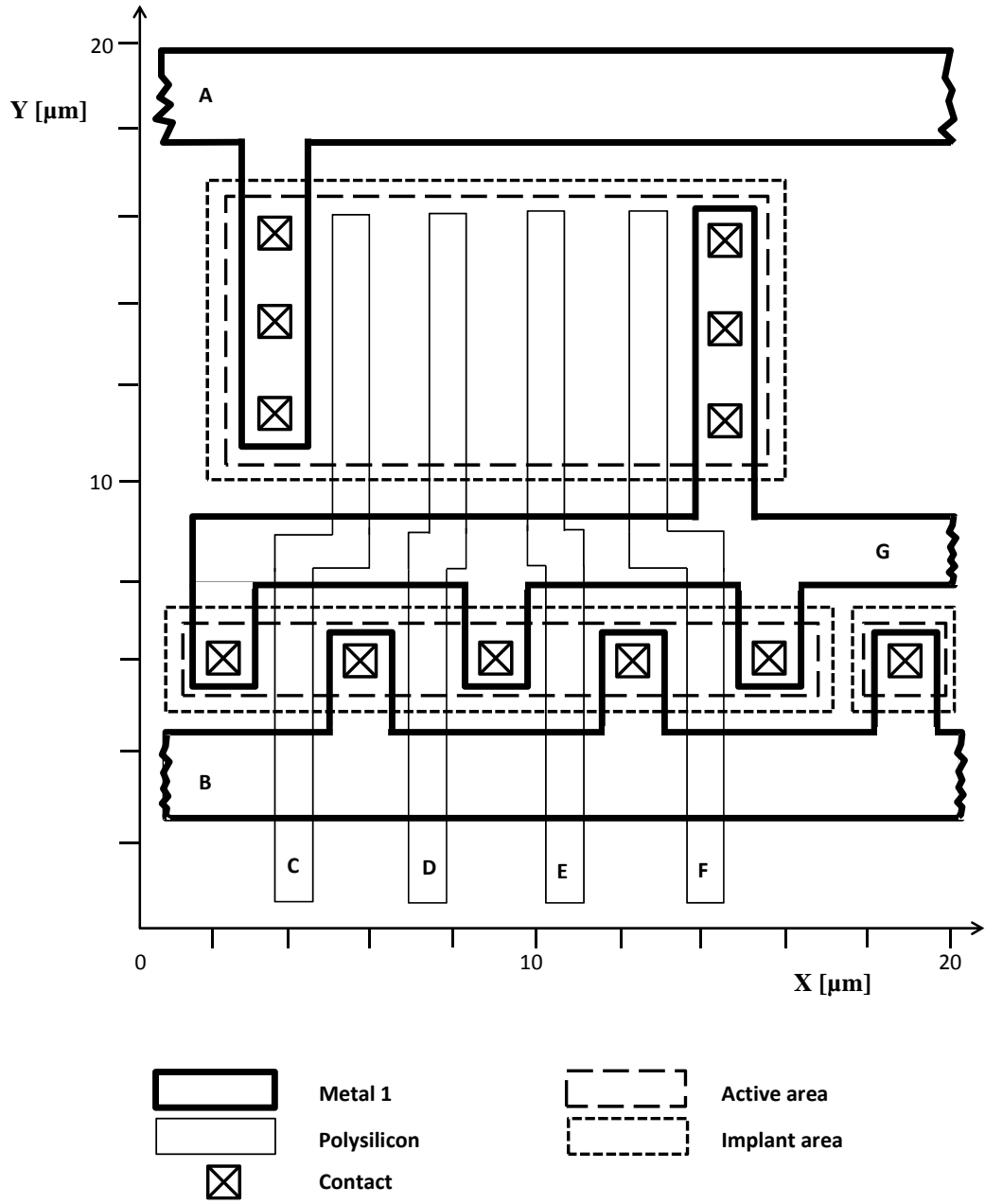
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Fig. 1

2   (a)   Give two main advantages and two disadvantages of the Silicon-On-Insulator (SOI) technology compared to bulk silicon technology.   [20%]

(b)   Describe schematically the process steps involved in producing Smart-Cut (Unibond) (SOI) wafers.   [20%]

(c)   The cross-section of a CMOS inverter cell made in a specialised Partial Silicon-On-Insulator technology is shown in Fig. 2.

(i)   What are the main advantages and disadvantages of using this technology against the typical Silicon-On-Insulator technology?   [10%]

(ii)   Using the answer sheet copy of Fig. 2, draw the equivalent circuit responsible for the latch-up, showing specifically the transistor terminals, the parasitic resistors and the connections between them. Which of the parasitic transistors is more likely to trigger the latch-up, and why?   Assume that the resistivity of the n-well is greater than that of the p-well.   [30%]

(iii)   State the static condition for the latch-up to occur as a function of the electrical parameters of the parasitic components.   [20%]

IN

V_{SS}

OUT

V_{DD}

| p+ | n+ | | n+ | | p+ | | p+ | n+ |

p well

n well
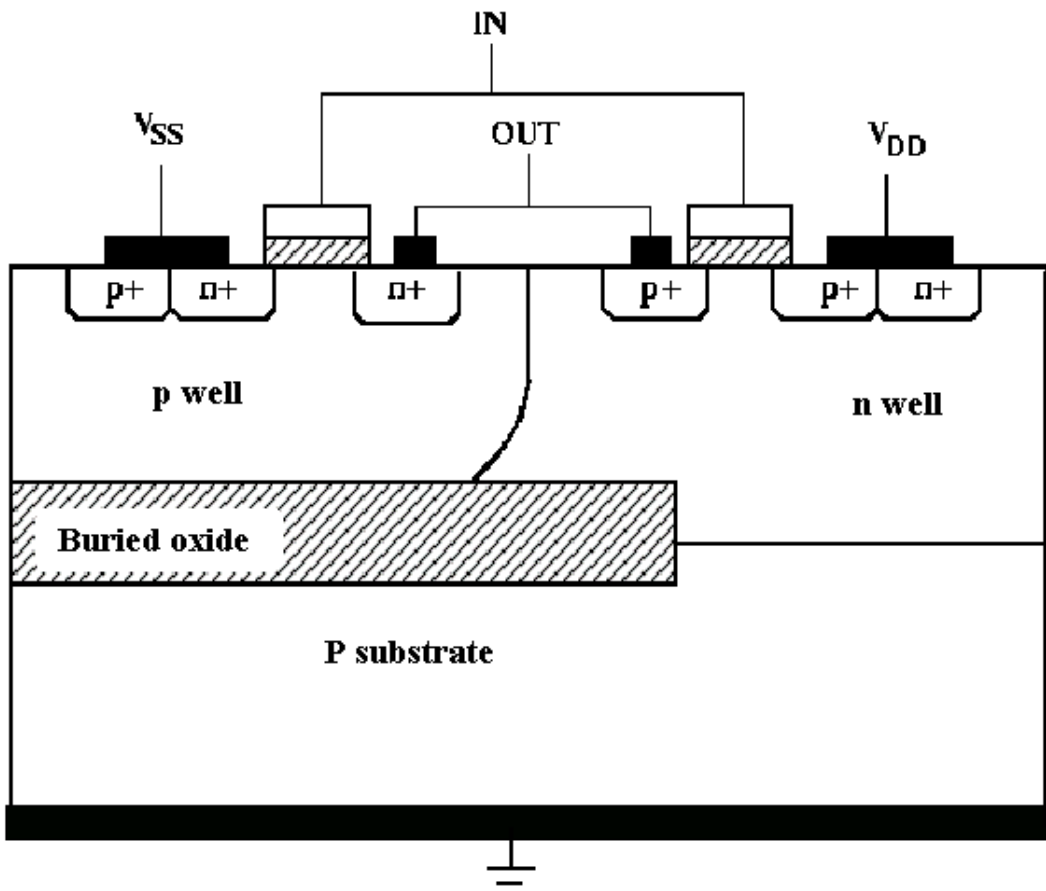
Buried oxide

P substrate

Fig. 2

3   (a) What is the meaning of the term *clock skew* in the context of VLSI designs using CMOS technology, and from what sources does it originate? Briefly discuss the measures that must be taken by IC designers to minimise the effects of clock skew in digital designs.   [30%]

(b) In a microcontroller circuit, a clock buffer distributes a single-phase clock signal to a remote part of the circuit by means of a bus consisting of uniform polysilicon interconnect.   The length and width of the interconnect are 10 mm and 1 μm respectively; the sheet resistance of the polysilicon is 40 Ω/square, and the capacitance per unit length is 2×10^{-10} F m^{-1}.

Estimate the delay incurred by the signal in propagating the length of the bus. Describe carefully how the delay would be affected if:

(i)   the width of the interconnect were doubled;   [20%]

(ii)   a *silicide* manufacturing process were used, reducing the sheet resistance of polysilicon to 4 Ω/square.   [20%]

(c) Inverting buffers are available with delay properties shown graphically and algebraically in Fig. 3. Suggest a suitable amendment to the original polysilicon bus arrangement in (b) that will reduce the delay by at least a factor 2, noting that a non-inverted clock is required at the remote end of the bus.   [30%]

Assume that the delay in each buffer depends only on the load capacitance it drives, and that all capacitances other than those due to interconnections can be ignored.

The following expression may be assumed for the propagation delay *T* of a pulse transmitted along a resistive conductor of length *l*:

$$T = 0.5 \; rcl^{2}$$

where *r* is the resistance per unit length, and *c* is the capacitance to substrate per unit length.
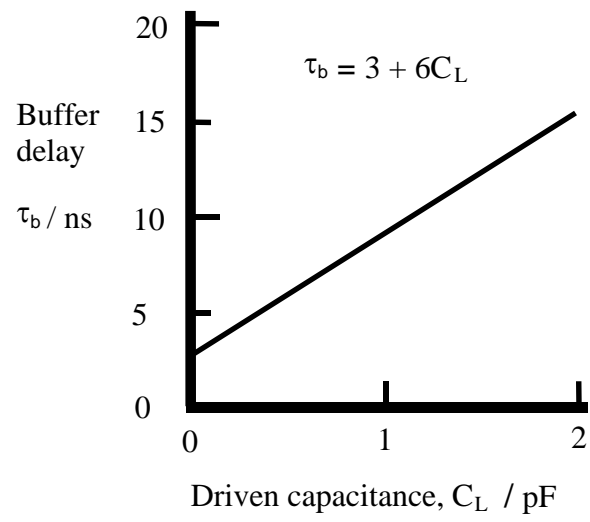
Fig. 3

4   A simple form of one-bit dynamic memory cell relying for its storage element on parasitic capacitance is shown in Fig. 4.

(a)   Briefly describe how this circuit works for *read* and *write* operations. Discuss the origin of capacitances C_S and C_B, and state how they affect the performance of the memory.   [40%]

(b)   A square array of cells based on the schematic in Fig. 4 is used as the basis of a memory chip operating from a 3 volt supply. Each cell occupies an area of the silicon wafer 2 μm × 2 μm. The capacitance C_S is 20 fF, and each transistor has drain-substrate capacitance of 5 fF. The metal interconnect used to form the bit line has specific capacitance per unit length of 0.5 fF μm^{-1}.

In this design, the maximum practicable size of the array is limited by charge-sharing effects which attenuate the signal being read out from an individual cell. If the sense amplifier used to read out the data is able to discriminate a signal at its input of 10 mV, estimate the largest memory that can be constructed using this cell. State any assumptions made.   [40%]

(c)   Explain how a design based on a trench capacitor or a stacked-capacitor structure might be used to enhance the charge sharing performance.   [20%]
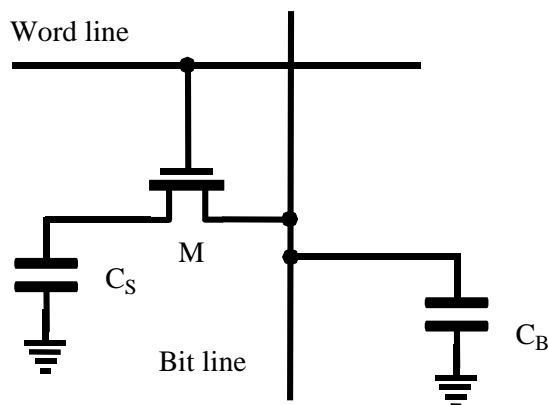

Fig. 4

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5   (a)   Describe the circuit structures used in CMOS technology to convey digital signals between input pads and the inputs of logic gates comprising small geometry devices. Discuss the precautions used to protect inputs from the effects of applying excessive voltages and static discharges, and to guard against latchup.   [50%]

(b)   A high voltage MOSFET fabricated in a 1 µm process has been estimated to have an average failure rate of 1×10^{-3} / h at an ambient temperature of 125 °C in a high temperature reverse bias (HTRB) test with 400 V applied across the drain-source terminals.

(i)   Describe briefly the general procedure for determining the activation energy, E_a , and the stress voltage coefficient, a.   [20%]

(ii)   Using the Arrhenius equation with temperature and voltage as stresses, estimate the average failure rate in the field of use where the ambient temperature is 40 °C and the line voltage is 200 V. Assume that the activation energy $E_a = 0.8$ eV and the stress voltage coefficient $a = 0.03$.   [30%]
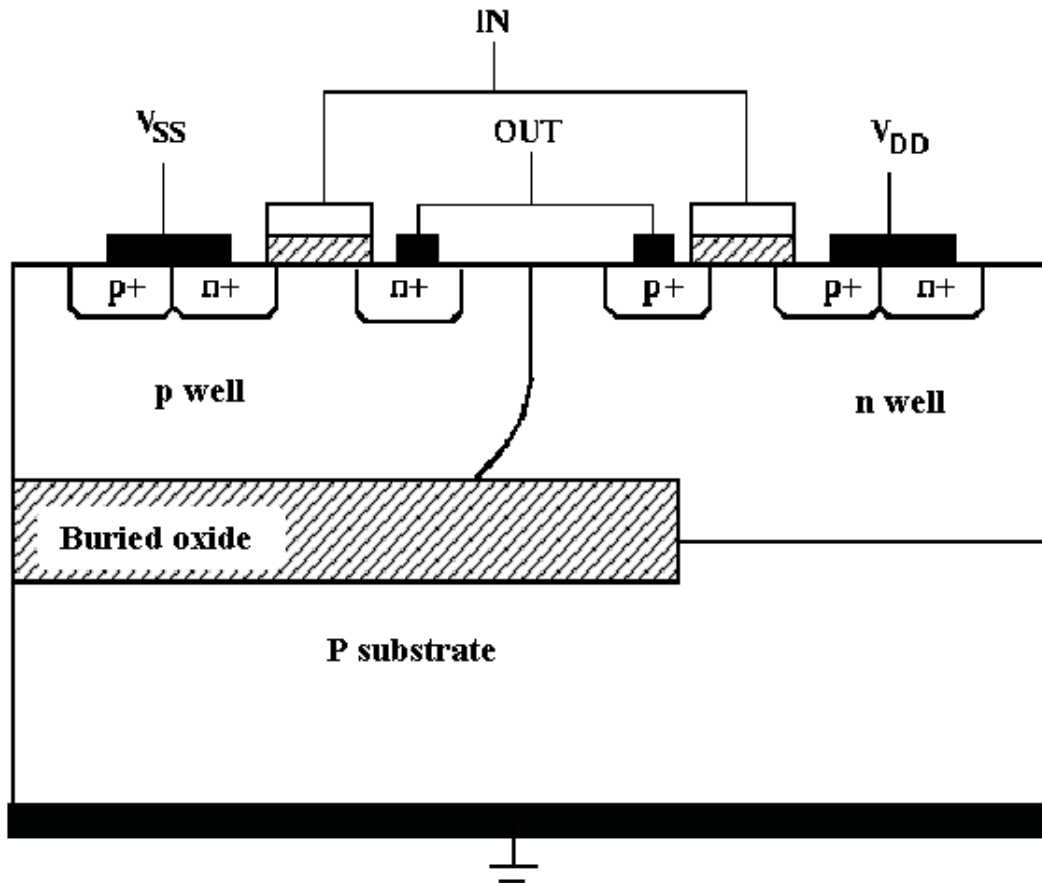
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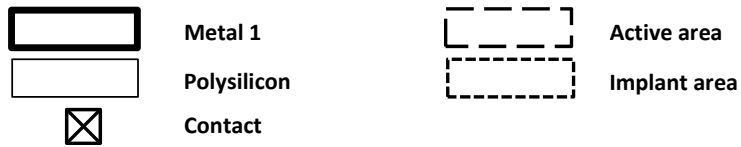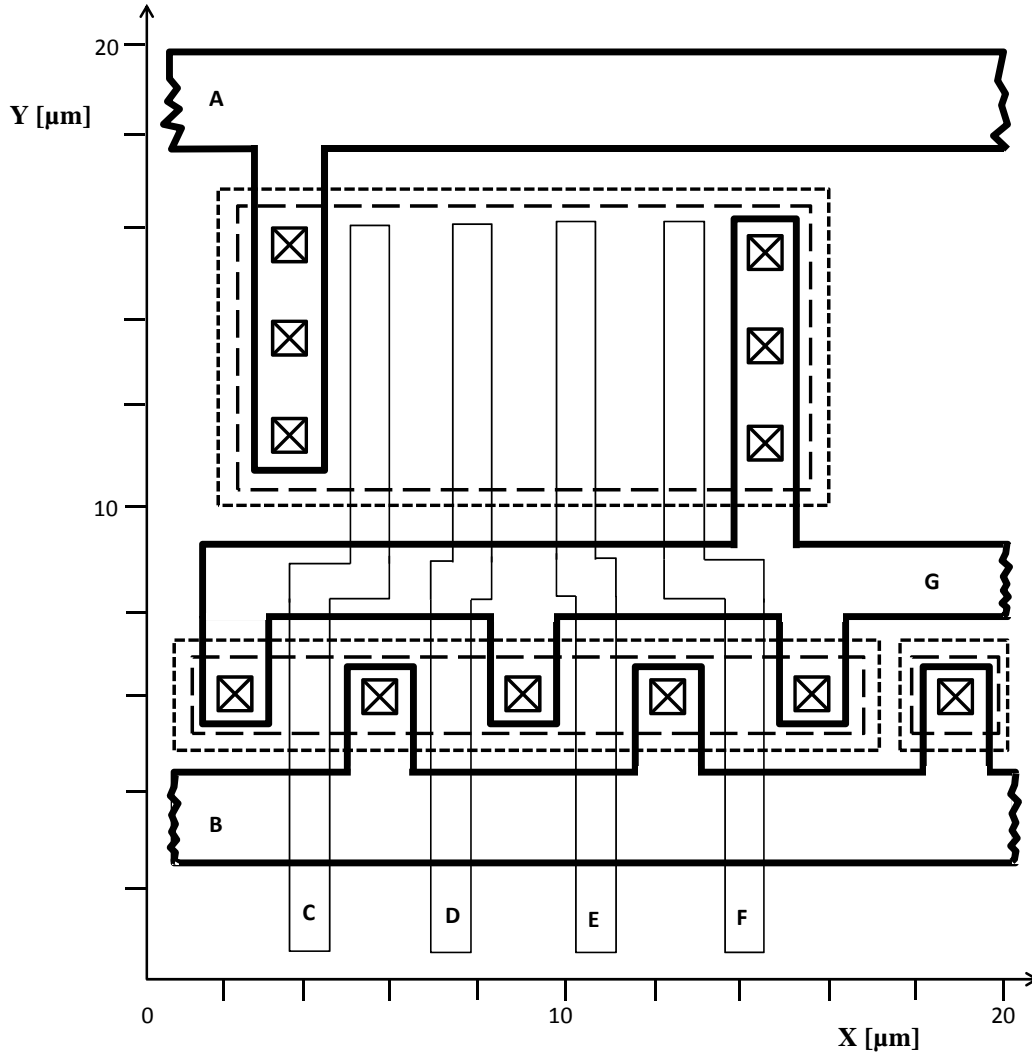
Additional copy of Fig. 1
(may be handed in with your script)

Candidate Number

IN

V_{SS}

OUT

V_{DD}

p+   n+   n+   p+   p+   n+

p well   n well

Buried oxide

P substrate

Additional copy of Fig. 2
(may be handed in with your script)

dmh05

4B7 VLSI Design, Technology and CAD   -   2013   Numerical Answers

1.

2.

3.

4.   (b) 500 × 500 bits approximately, or 250 kbits.

5.   (b) 4.4 FIT