Version FU/3

EGT3
ENGINEERING TRIPOS PART IIB

Tuesday 23 April 2019 2 to 3.40

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Draw schematically the structure of a superjunction MOSFET. Draw schematically two graphs, the first showing the horizontal component of the electric field as a function of the horizontal distance and the second showing the vertical component of the electric field as a function of the vertical distance. Two curves should be shown on each graph corresponding to the breakdown voltage and a voltage level at which the superjunction structure is not completely depleted. [40%]

(b) Either a power MOSFET or an Insulated Gate Bipolar Transistor (IGBT) are to be used in an inductive application with the current and voltage turn-off waveforms shown schematically in Figure 1. The rail voltage V_{dc} = 400V and the on-state current required for the application is I_{ON} = 3A. The static and dynamic parameters of the two transistors are summarised in Table 1. Consider the turn-on and the off-state losses to be negligible for both transistors. The switching frequency is variable from 10 kHz to 100 kHz with a constant duty cycle D = 50%.

Parameter	On-state voltage drop V_{ON} [V]	Turn-off delay time t_s [μs]	Turn-off voltage growth time t_g [μs]	Turn-off current fall time t_f [μs]
Power MOSFET	5	0.1	0.3	0.1
IGBT	2	0.1	0.3	0.6

Table 1

(i) Estimate the total power losses in the Power MOSFET and the IGBT and sketch a graph of these as a function of frequency. Comment on the efficiency of these transistors and the preferred use of one or the other for the given range of frequency. [40%]

(ii) The parameters in Table 1 are given at room temperature. How would you expect the on-state and the turn-off power losses to change at higher junction temperatures for the two transistors? Will the junction temperature influence the choice of the transistor? [20%]

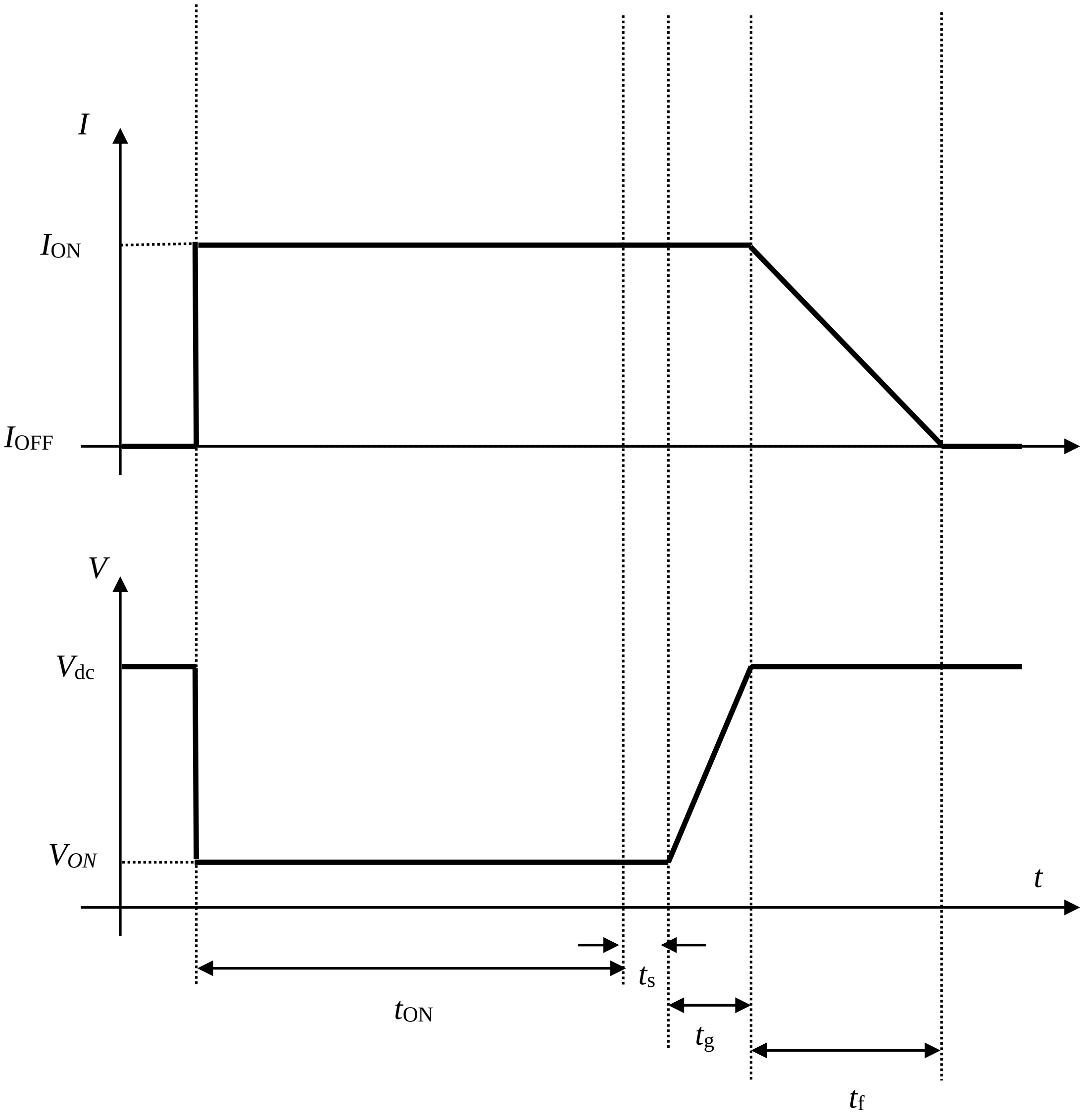

Figure 1

2 (a) Explain the dV/dt effect in thyristors. Give two solutions to improve the dV/dt ratings and discuss their advantages and disadvantages. [30%]

(b) (i) Using the simplified Ebbers-Moll equivalent models for the two bipolar transistor components of the thyristor, find an expression for the anode current in the voltage blocking mode as a function of the leakage currents of the bipolar transistors and their current gains α_{npn} and α_{pnp}. [30%]

(ii) Calculate the break-over voltage, V_{BO}, of the thyristor, assuming that $\alpha_{npn}= 0.5$ remains constant. The width of the n- drift region is $w_{drift} = 200$ μm, the hole diffusion length $L_p = 50$ μm and the doping concentration of the drift region, $N_D= 10^{13}$ cm^{-3}. [30%]

(iii) Discuss briefly the occurrence of break-over and avalanche breakdowns in the drift region of a thyristor and in the drift region of an Insulated Gate Bipolar Transistor (IGBT). [10%]

You may assume the following equations in the calculations of breakdown and current gain of a pnp transistor

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

$$\alpha_{pnp} \approx 1 - \frac{{w_{eff}}^2}{2{L_p}^2}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, α_{pnp} is the current gain of the pnp transistor, w_{eff} is the effective base width of the pnp transistor, L_p is the hole diffusion length, q is the electronic charge and the other symbols have their usual meaning. $\varepsilon_0 = 8.854 \times 10^{-12}$F/m, $\varepsilon_r = 11.9$ for Silicon.

(cont.

3 The structure in Figure 2 is a lateral power device.

(a) Explain briefly its operation during the forward on-state, off-state, turn-on and turn-off. [40%]

(b) Draw an equivalent circuit for the device. Explain what would be an appropriate bias for the substrate terminal. [25%]

(c) Explain the operation of this device in a reverse on-state mode (when the cathode potential is higher than the anode potential). [10%]

(d) The device in Figure 2 is based on a lateral planar technology. Draw the cross-section of an equivalent device using a vertical technology with a trench gate. Give one advantage and one disadvantage of the vertical structure compared to the lateral structure. [25%]

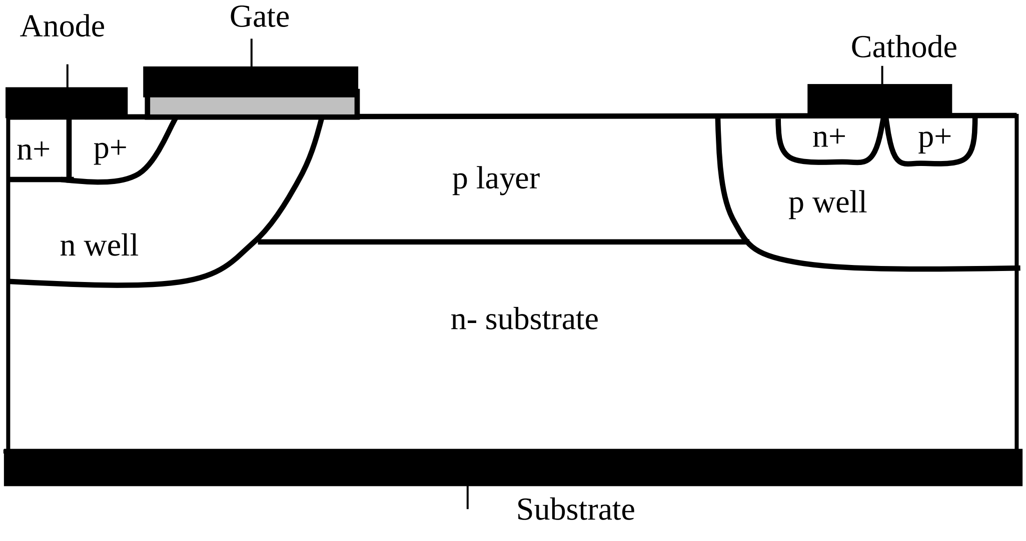

Figure 2

4 (a) Draw schematically two AC to DC converters, first using linear electronics (LE) and second using switch mode power electronics (SMPS). Describe their operation and discuss their relative advantages and disadvantages. [40%]

(b) Using a simplified equivalent circuit find the output voltage as a function of the rectified input voltage, the duty cycle and the turns ratio of the transformer for the AC to DC SMPS converter. State any assumptions made. [30%]

(c) Explain the role of the feedback circuit in a flyback AC to DC SMPS controller. [10%]

(d) Explain briefly the performance of a superjunction compared to that of a Power MOSFET in an AC to DC power supply as a function of frequency, temperature, and power. [20%]

END OF PAPER