

Monday 8 June 2015 9 to 12

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**Paper 3**

**ELECTRICAL AND INFORMATION ENGINEERING**

Answer *all* questions.

The *approximate* number of marks allocated to each part of a question is indicated in the right margin.

Answers to questions in each section should be tied together and handed in separately.

Write your candidate number **not** your name on the cover sheet.

**STATIONERY REQUIREMENTS**

Single-sided script paper

**SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM**

Engineering Data Book

CUED approved calculator allowed

**10 minutes reading time is allowed for this paper.**

**You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.**

**SECTION A**

1 (long) The FET amplifier shown in Fig. 1 is to be biased so that  $V_{GS} = -2$  V,  $V_{DS} = +8$  V and  $I_D = 4$  mA. At this operating point, the FET has small-signal parameters of  $g_m = 5$  mA V<sup>-1</sup> and  $r_d = 10$  k $\Omega$ .

- (a) Explain how the resistor chain on the left of the FET sets the operating point of the FET. [4]
- (b) Determine the values of  $R_1$  and  $R_2$  to achieve the desired operating point. [4]
- (c) Draw a small-signal equivalent circuit for the amplifier circuit of Fig. 1, valid for mid-band frequencies. Hence determine the small-signal gain and the output impedance of the circuit. [10]
- (d) The low frequency half-power frequency of the amplifier is dominated by the effect of  $C_0$ , and is designed to be 10 Hz. With a load resistor of 5 k $\Omega$  connected between points A and B, determine the value of  $C_0$ . [8]
- (e) Given the choice of gate-source voltage of  $-2$  V, explain why  $V_{DS} = 12$  V is the optimum choice of the drain-source voltage. [4]

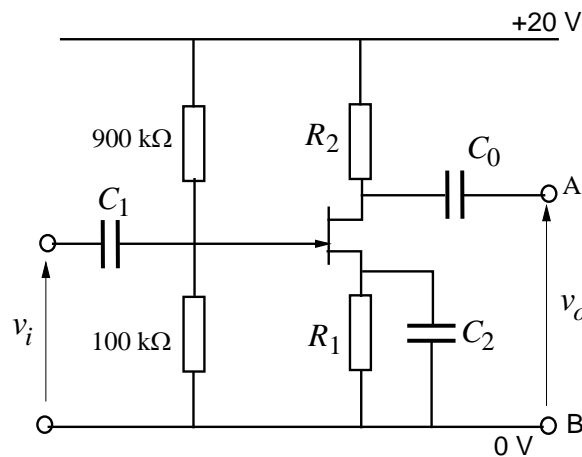


Fig. 1

2 (long) Consider the amplifier circuit in Fig. 2.

(a) At a mid-band frequency, where  $C_1$  may be considered to be an open circuit, calculate the value of  $R_2$  required to give a voltage gain of 300 between input and output. The operational amplifier may be considered ideal. [8]

(b) What is the mid-band input impedance of the circuit? [6]

(c) Calculate the value of  $C_1$  required to give a 3 dB high frequency cut-off at 10 kHz, where the circuit gain drops to  $1/\sqrt{2}$  of its mid-band value. [6]

(d) In practice, the operational amplifier has an open-loop voltage gain of 20 000, but is otherwise ideal. What is the actual mid-band voltage gain in dB when the circuit drives a load impedance of  $25 \Omega$ ? [10]

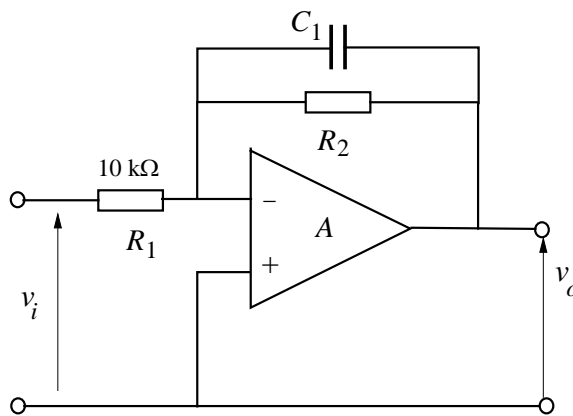


Fig. 2

3 (short) Fig. 3 shows an AC circuit connected to a 240 V, 50 Hz power supply. Determine the total complex impedance of the circuit and hence find the magnitude and phase of the input current with respect to the voltage source. [10]

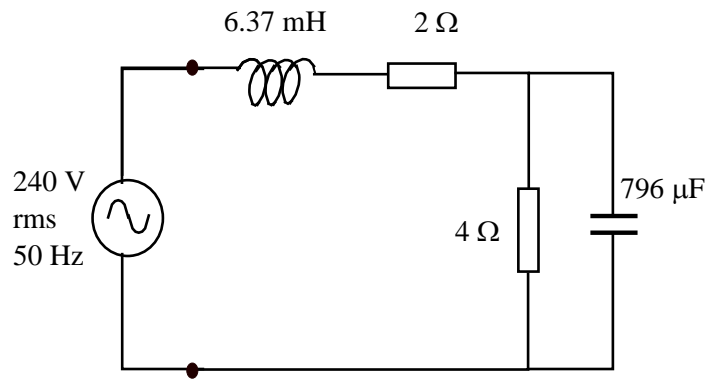


Fig. 3

4 (short) In the circuit of Fig. 4, the op-amp is ideal except for its finite gain,  $A$ . Derive an expression for the gain of the circuit,  $v_o / v_i$  and show that as  $A$  tends to infinity, the gain of the circuit tends to

$$\frac{v_o}{v_i} = 1 + \frac{R_1}{R_2}$$

[10]

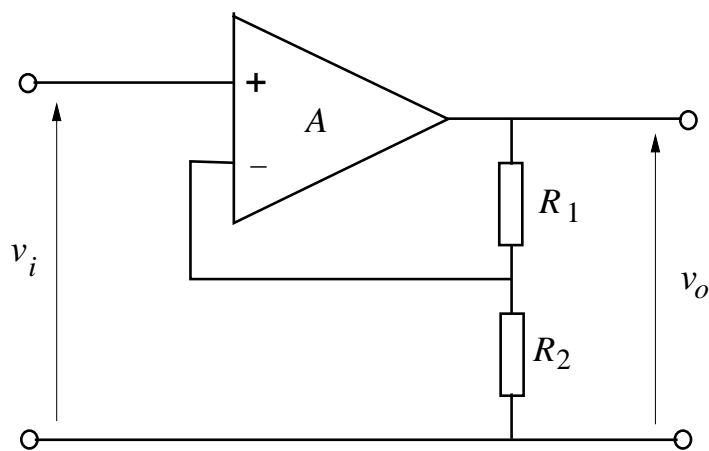


Fig. 4

5 (short) Using Thévenin's theorem or otherwise, determine the current flowing in the  $2\ \Omega$  resistor in the circuit of Fig. 5. [10]

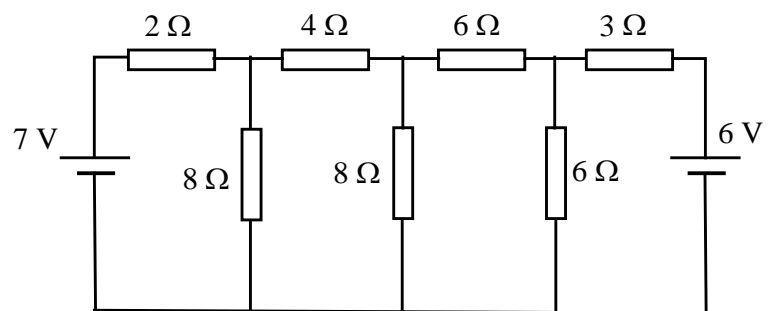


Fig. 5

## SECTION B

6 (short)

(a) Describe what is meant by 2's-complement representation of a binary number and explain its significance in digital information processing. [2]

(b) Design a circuit that converts a 3-bit binary 2's-complement number  $X$  to its negative  $-X$ , represented as a binary number in 2's-complement form. The circuit should be composed only of NAND gates and the smallest possible number of such gates should be used. [8]

7 (short)

- (a) Draw a circuit showing how an SR bistable can be constructed by means of only 2-input NAND gates. Write Boolean expressions relating the outputs and inputs of the bistable. [2]
- (b) Describe the features of a JK bistable that are not present in an SR bistable and discuss in what ways these are advantageous. [4]
- (c) In an SR bistable the inputs  $S$  and  $R$  have values  $S = R = 1$  and these then change to  $S = R = 0$ . Explain how the outputs of the bistable would behave. [4]



8 (short)

(a) Describe the operation of a tri-state buffer and explain how this is used to facilitate read/write operations from the memory of a microprocessor. [4]

(b) Consider the following commands in assembly language for the PICF675 processor:

```
        movlw 0xAA
        movwf 0x35
        decf 0x35
label   decfsz 0x35
        goto label
```

Explain the operation of each of the commands.

Calculate the number of cycles taken for the commands to execute.

Calculate the number of cycles taken if, instead, the following commands are executed:

```
        movlw 0xAA
        movwf 0x35
label   decf 0x35
        decfsz 0x35
        goto label
```

[6]

9 (long)

(a)  $X$  and  $Y$  are two 2-bit unsigned binary numbers, where  $Y > 1$ . The 4-bit binary number  $P$  satisfies the equation

$$P = (X)^2 + Y$$

Design a digital circuit that evaluates the most significant bit and the least significant bit of  $P$  from the bits of  $X$  and  $Y$ . The circuit should be composed only of NOR gates and the smallest possible number of such gates should be used.

Explain why designs with larger numbers of gates can be beneficial. [15]

(b) 2-bit binary unsigned numbers are received sequentially by a detector. Each of these numbers is greater than 1. The output  $Z$  of the detector becomes 1 if the current value of the number received is greater than 2 and the value of the previous number received was equal to 2. The output  $Z$  is otherwise 0.

(i) Draw a state diagram for the system. [6]

(ii) State how many JK bistables will be needed to implement the detector and draw a state transition table (assume that unused states are never reached). [5]

(iii) Derive simplified Boolean expressions for the J inputs of the bistables. [4]

## SECTION C

10 (short)

(a) Derive the expression  $C = \epsilon A/d$  for a parallel plate capacitor, defining each of the symbols in the expression. [4]

(b) As shown in Fig. 6, a capacitor is made with a solid-foam dielectric of thickness  $d$  and relative permittivity  $\epsilon_r = 1$ . The fixed top electrode is a sheet of metal glued to the dielectric. The bottom electrode is a metal sheet which is attracted to the bottom face of the dielectric by the electric field, applied by thin, light and flexible wires. Find an expression for the minimum voltage  $V$  that must be applied if the metal sheet, of density  $\rho$  per unit area, is not to fall from the dielectric. [6]

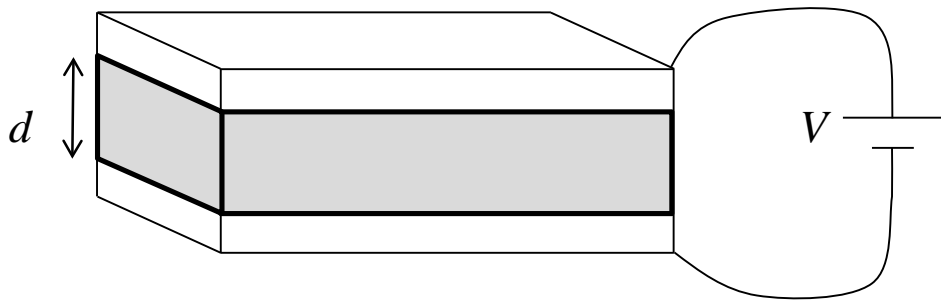


Fig. 6

11 (long)

(a) As shown in Fig. 7(a), a closed ring of soft cast-steel has a coil of insulated wire wound round it a total of  $N$  times, carrying a current  $I$ . When considering the magnetic induction in the ring, explain whether or not it matters if the winding is uniform round the ring or concentrated over one segment. [4]

(b) Suppose the ring has a cross-sectional area of  $1000 \text{ mm}^2$  and a mean circumference of  $600 \text{ mm}$ . Find the number of ampere-turns required to produce a magnetic flux density of  $B = 1 \text{ T}$  inside the ring. The relevant  $B$ - $H$  curve for cast-steel is given in Fig. 8. [7]

(c) A cut is made through the ring leaving a gap of  $2 \text{ mm}$  as shown in Fig. 7(b). Find the number of ampere-turns required to produce the magnetic flux density of  $B = 1 \text{ T}$ . Explain the difference between this answer and that in part (b) above. [8]

(d) The effect of the magnetic field is to exert forces that would tend to close the gap. Estimate the force that would need to be applied to keep the gap at  $2 \text{ mm}$ , making explicit any approximations made. [8]

(e) How is the gap maintained in practice? [3]

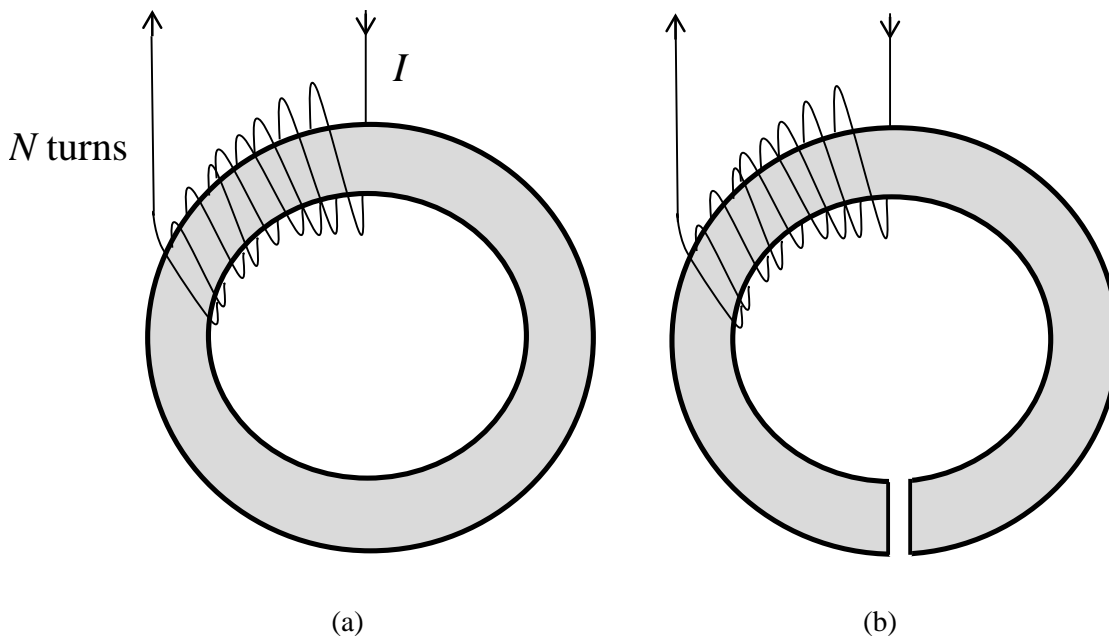


Fig. 7

cont.

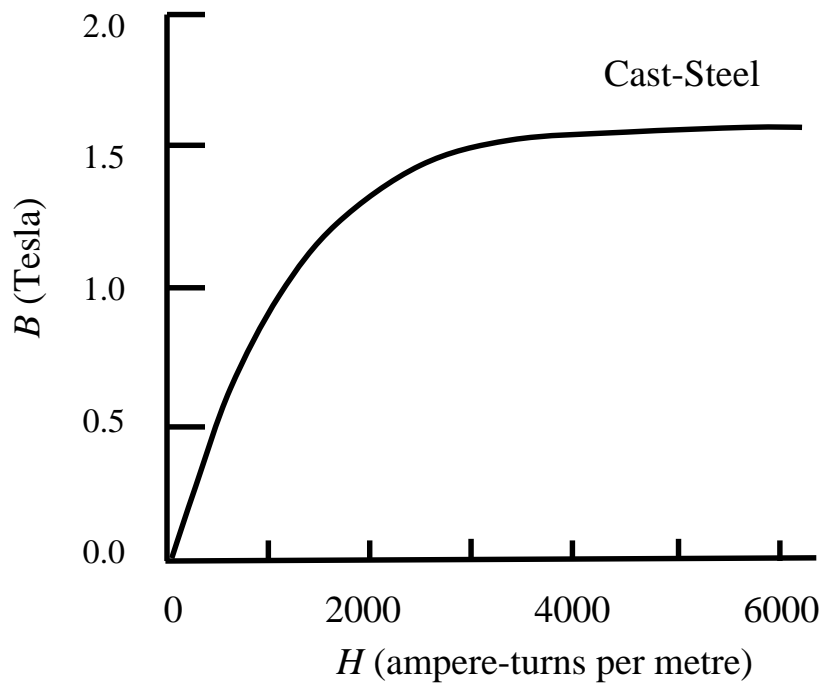


Fig. 8

12 (short)

(a) Use Ampère's law to derive an expression for the magnetic field intensity  $B$  at a distance  $d$  from an infinite straight wire carrying a current  $I$ . [5]

(b) As shown in Fig. 9, three orthogonal wires are each carrying a current  $I$  and cross without touching. Using the coordinate system in Fig. 9, and assuming that the currents flow in the positive directions, what is the magnetic field strength and direction at each of the four points  $(d, d, d)$ ,  $(-d, -d, -d)$ ,  $(d, d, 0)$  and  $(-d, -d, 0)$ , where  $d > 0$  ? [5]

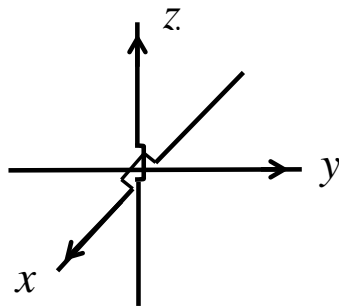


Fig. 9

**END OF PAPER**

## Answers

### Section A

Q1. (b)  $R_1 = 1 \text{ k}\Omega$ ,  $R_2 = 2 \text{ k}\Omega$ ; (c) gain =  $-8.33$ ,  $R_{\text{out}} = 1.67 \text{ k}\Omega$ ; (d)  $C_0 = 2.39 \times 10^{-6} \text{ F}$

Q2. (a)  $R_2 = 3 \text{ M}\Omega$ ; (b)  $R_{\text{in}} = 10 \text{ k}\Omega$ ; (c)  $C_1 = 5.3 \text{ pF}$ ; (d) gain = 296

Q3.  $Z_{\text{tot}} = 4 \Omega$ ,  $I = 60 \text{ A}$

Q5.  $I = 1 \text{ A}$

### Section B

Q6. (b)  $Z_1 = Y_1$ ,  $Z_2 = Y_2 \bar{Y}_1 + \bar{Y}_2 Y_1$ ,  $Z_3 = Y_2 \bar{Y}_3 + Y_1 \bar{Y}_3 + Y_3 \bar{Y}_2 \bar{Y}_1$ ,  $Z_4 = Y_2 \bar{Y}_3 + Y_1 \bar{Y}_3$

Q7. (a)  $Q_1 = S + \bar{Q}_2$ ,  $Q_2 = R + \bar{Q}_1$

(b) master/slave configuration with clock, preset/clear, inputs both 1 toggles output

(c) depends on the delays present

Q8. (b) 509 cycles, 341 cycles

Q9. (a)  $P_4 = \overline{\overline{X_1 + X_2}}$ ,  $P_1 = \overline{\overline{\overline{X_1 + Y_1} + \overline{X_1 + Y_1}}}$

(b)  $J_A = X_1 Q_B$ ,  $J_B = \bar{X}_1$

### Section C

Q10. (b)  $V > d[2\rho g/\epsilon_0]^{1/2}$

Q11. (b)  $H = 1000 \text{ A}\cdot\text{m}^{-1}$ , 600 A.turns; (c) 2188 A.turns; (d) 398 N

Q12. (b)

$(d, d, d)$   $\mathbf{B} = B_d(0, 0, 0)$

Magnitude: 0

$(-d, -d, -d)$   $\mathbf{B} = B_d(0, 0, 0)$

Magnitude: 0

$(d, d, 0)$   $\mathbf{B} = B_d(-1/2, 1/2, 0)$

Magnitude:  $B_d/\sqrt{2}$

$(-d, -d, 0)$   $\mathbf{B} = B_d(1/2, -1/2, 0)$

Magnitude:  $B_d/\sqrt{2}$