Version FU/3

EGT2
ENGINEERING TRIPOS PART IIA

Friday 1 May 2015 9.30 to 11

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Describe what is meant by the term *saturation* when it refers to:

(i) MOS transistors; [15%]

(ii) bipolar transistors [15%]

in the context of logic gates made from these devices. Your answer should clearly indicate instances where saturation can be used to advantage in the design of logic gates, and where it is disadvantageous.

(b) Fig. 1(a) shows a logic gate based on MOS transistors M1 and M2 whose device transconductances k_1 and k_2 are shown. Calculate the logic 'low' output voltage V_{OL} for this gate assuming the threshold voltage for both transistors $V_T = 1$ V, and input voltage $V_I = 6$ V when $V_{OUT} = V_{OL}$. Indicate clearly which device, if any, is in its saturation mode. [40%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T);$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T),$$

where k is the device transconductance parameter, and other symbols have their usual meanings.

(c) For the bipolar transistor inverter circuit shown in Fig. 1(b), the value of σ, the degree of saturation for the circuit, is 0.2. Explain the significance of this value. If the values of $V_{CE\,sat}$ and $V_{BE\,sat}$ for the device are 0.1 V and 0.7 V respectively, calculate for this circuit the input voltage V_B expected to produce this value of σ. [30%]

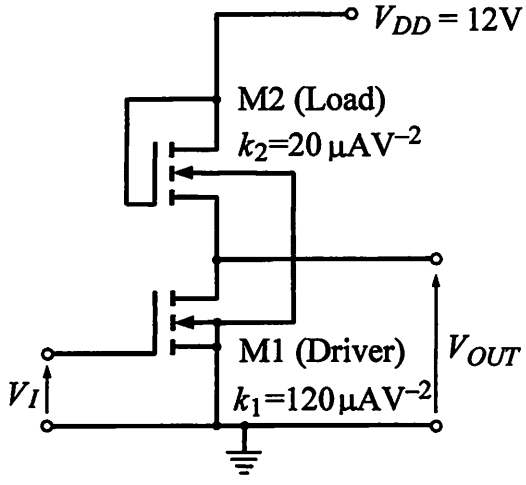

Fig. 1(a)

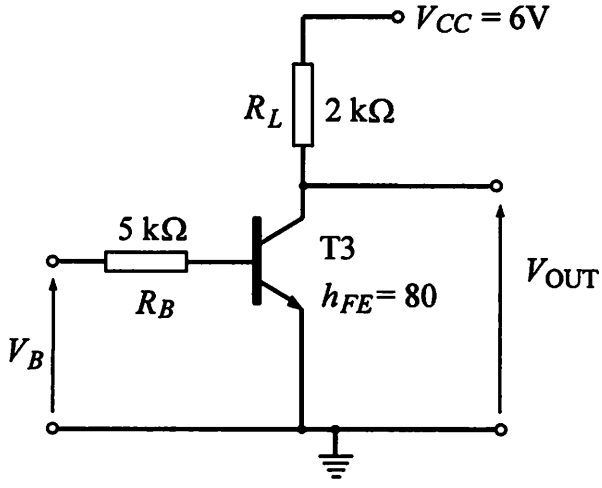

Fig. 1(b)

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2 (a) In the Quine-McClusky tabular method give the definition of *prime implicants* and briefly explain the use of the *prime implicant table*. Explain why if a logic expression is not in a canonical form, or is not brought to a canonical form, the Quine-McClusky tabular method may not always give an optimally simplified solution. [20%]

(b) Implement the following logic function:

$$T = \Sigma\,(0,4,8,11,13,15)$$

using a multiplexer and show the circuit implementation. [30%]

(c) Fig. 2 shows a sequential system containing a counter, a start-up circuit logic gates, and a *Light Emitting Diode* (LED). There are two push buttons that determine the 'START' and the 'RESET' of the circuit

(i) Describe the operation of the various blocks in the circuit and determine the basic function that the circuit performs when the 'START' button is pressed. Why does the circuit require a 'RESET' button? [30%]

(ii) If the on-state voltage drop across the LED is 1.7 V determine the maximum current that needs to be absorbed by the NAND gate. [20%]

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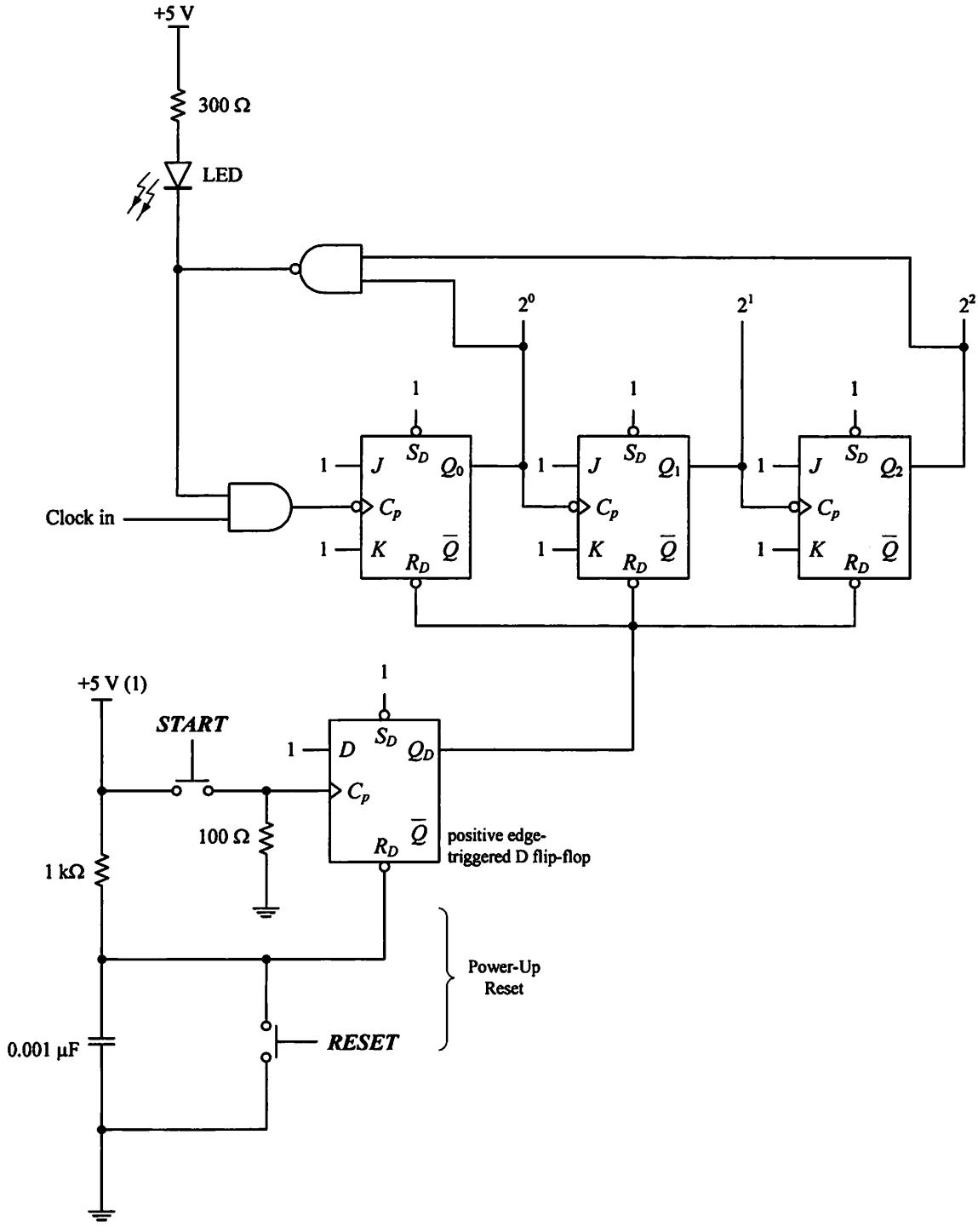

Fig. 2

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3 (a) Briefly discuss the advantages and disadvantages of implementing logic functions with *ROMs, Multiplexers and PLAs.* [20%]

(b) The diagram of a vending machine that dispenses four drinks, coffee (COFFEE), Hot chocolate (HOT), Tea (TEA) and Cappuccino (CAP) is shown in Fig. 3. The machine has a single coin slot and accepts 10p and 5p, one coin at a time. When 15 pence is received the drink dispensing mechanism (DISPENSE) is activated. As a result one of the four drinks is released as a function of the control inputs A and B (from the keypad) as shown in Table 1. For simplicity assume that the user selects the type of drink before inserting any coins. State any other assumptions made.

(i) Design the Control Logic in Fig. 3 for the vending machine that dispenses a drink for 15 pence in coins and selects one of the 4 outputs as shown in table 1. Draw the state diagram and state table showing the allocation of states. [30%]

(ii) Draw the circuit implementation of the control using a single PLA and D bistables. [30%]

(iii) Comment on the existence of essential hazards, if any, in the implemented circuit. [20%]

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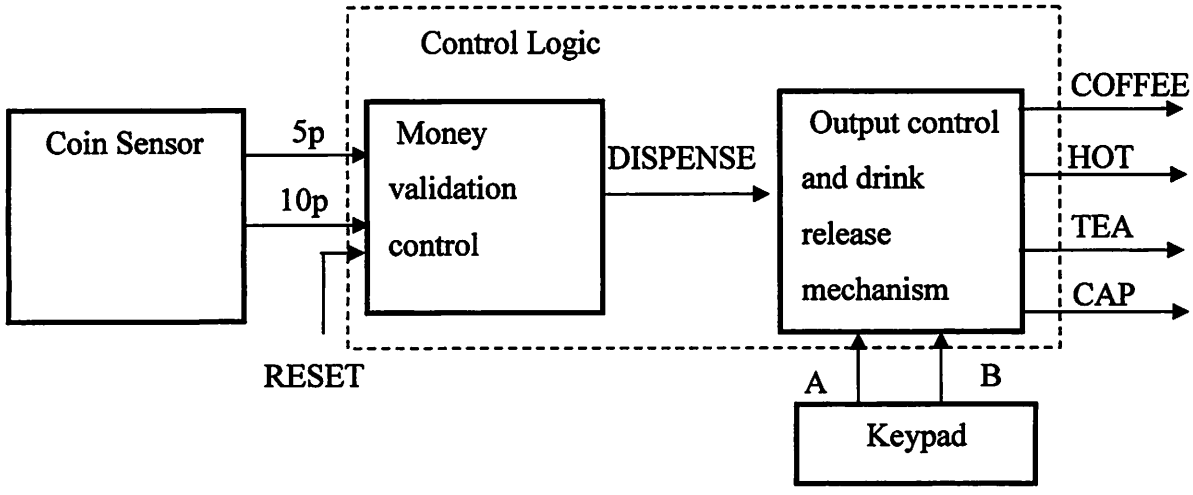

Fig. 3

INPUTS AB	OUTPUTS
00	COFFEE
01	HOT (CHOCOLATE)
10	TEA
11	CAP(PUCCINO)

Table 1

4 (a) Compare the advantages and disadvantages of the major digital logic families based on MOS and bipolar devices. In your account indicate briefly under what circumstances each family can provide desirable properties. Why has CMOS technology emerged as the most popular choice? [40%]

(b) Fig. 4 shows the schematic diagram of a simple static random-access memory cell.

(i) Explain briefly the mode of operation of this circuit, and describe the role of the signals *word*, *bit*, and $\overline{bit}$ in allowing data to be written and read. [25%]

(ii) What special measures need to be taken in the design of the inverters A and B to allow the circuit to work correctly? [15%]

(iii) With the help of a suitable block diagram, describe the additional circuit elements necessary to allow the cell to be interfaced to an external circuit. [20%]

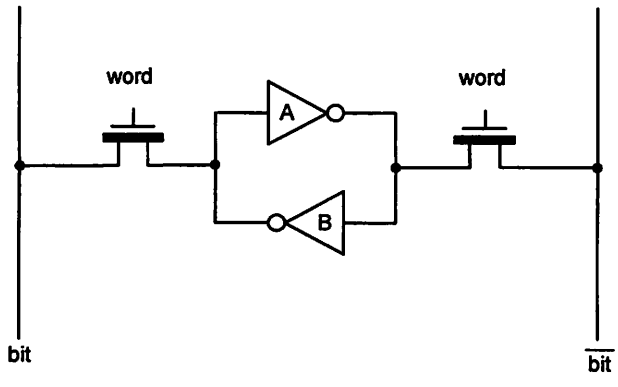

Fig. 4

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