

EGT2
ENGINEERING TRIPOS PART IIA

Thursday 21 April 2016 9.30 to 11

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed

Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Give the reasons for the popularity of CMOS technology in the design of digital logic systems. What are the disadvantages of CMOS? Your answer should include references to: implementation, compactness, input and output levels, and drive capability, as well as any other factors you consider important. [30%]

(b) Two MOS transistors with channel lengths L_1 and L_2 and equal channel widths W are connected in series, and have their gate electrodes connected together as shown in Fig. 1(a). Show that the two transistors acting together in non-saturation mode have a current-voltage characteristic that is the same as that of a single transistor with channel length equal to $L_1 + L_2$. You may neglect the body effect, but state any other assumptions made. [40%]

(c) Fig. 1(b) shows a two-input NAND gate implemented as a CMOS circuit using MOS transistors with channel dimensions W/L as indicated. Determine the supply current drawn if inputs A and B are linked together and connected to a supply of 1.5 V. Take $V_{DD} = 3$ V, $V_{TN} = 0.5$ V, $V_{TP} = -0.5$ V and $k = k' W / L$, where $k'_N = 8 \mu\text{A}/\text{V}^2$ and $k'_P = 4 \mu\text{A}/\text{V}^2$.

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2], \quad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2} (V_{GS} - V_T)^2, \quad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance. [30%]

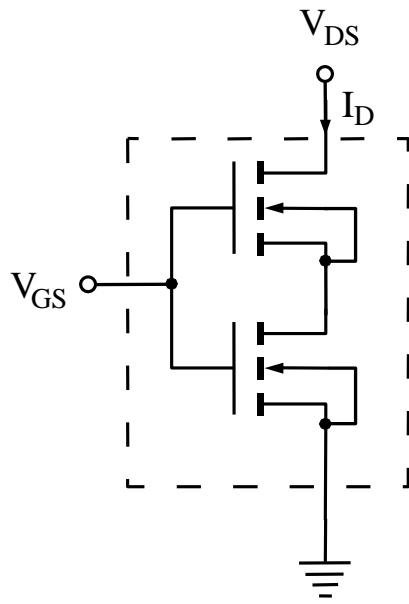


Fig. 1(a)

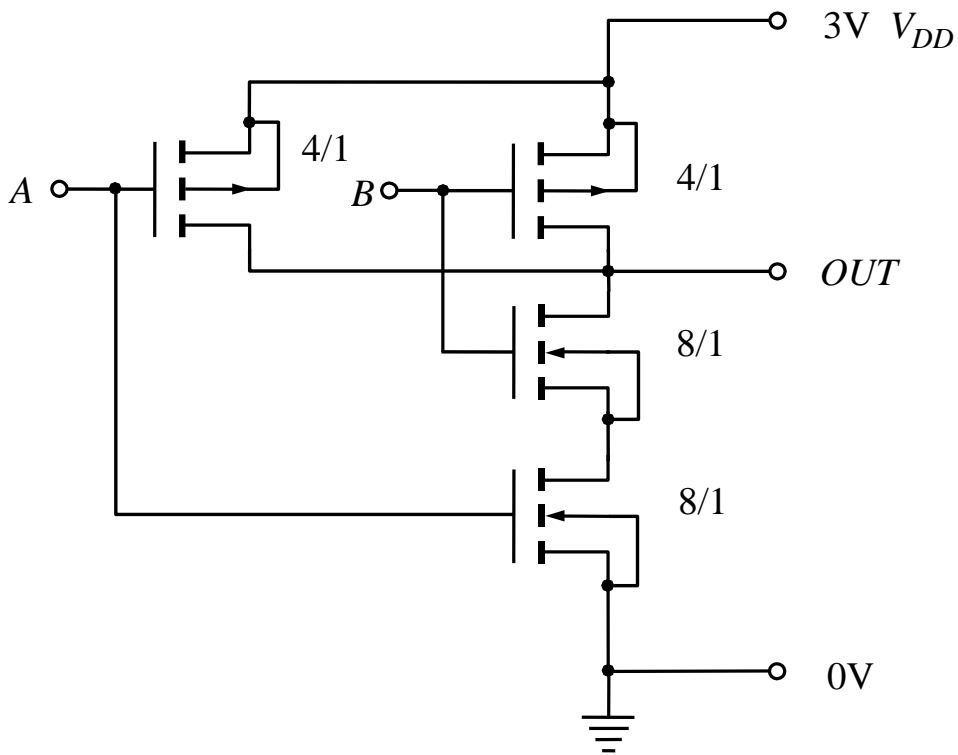


Fig. 1(b)

2 (a) Briefly describe the principles of operation of a Schmitt inverter. Sketch a graph depicting a typical voltage transfer characteristic for a Schmitt inverter, and indicate the *output high-to-low transition*, the *output low-to-high transition* and the *hysteresis*. What is the significance of these three terms? [30%]

(b) How might such a gate be used to receive digital signals transmitted along a cable of significant length, and what advantages would this be expected to give? [20%]

(c) Fig. 2 shows the circuit schematic for a Schmitt inverter implemented as a CMOS circuit using MOS transistors PI , PO , PF , NI , NO and NF . The six transistors have corresponding device transconductances k_{PI} , k_{PO} , k_{PF} , k_{NI} , k_{NO} and k_{NF} . You may assume that all three NMOS transistors have threshold voltage V_{TN} and all three PMOS transistors have threshold voltage V_{TP} .

Explaining your reasoning carefully, determine the values of V_{OH} and V_{OL} expected at the output with normal logic levels applied at the input. [30%]

(d) Explain why it is desirable to buffer the output of such a gate, and indicate how this might be achieved. [20%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2], \quad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2} (V_{GS} - V_T)^2, \quad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance.

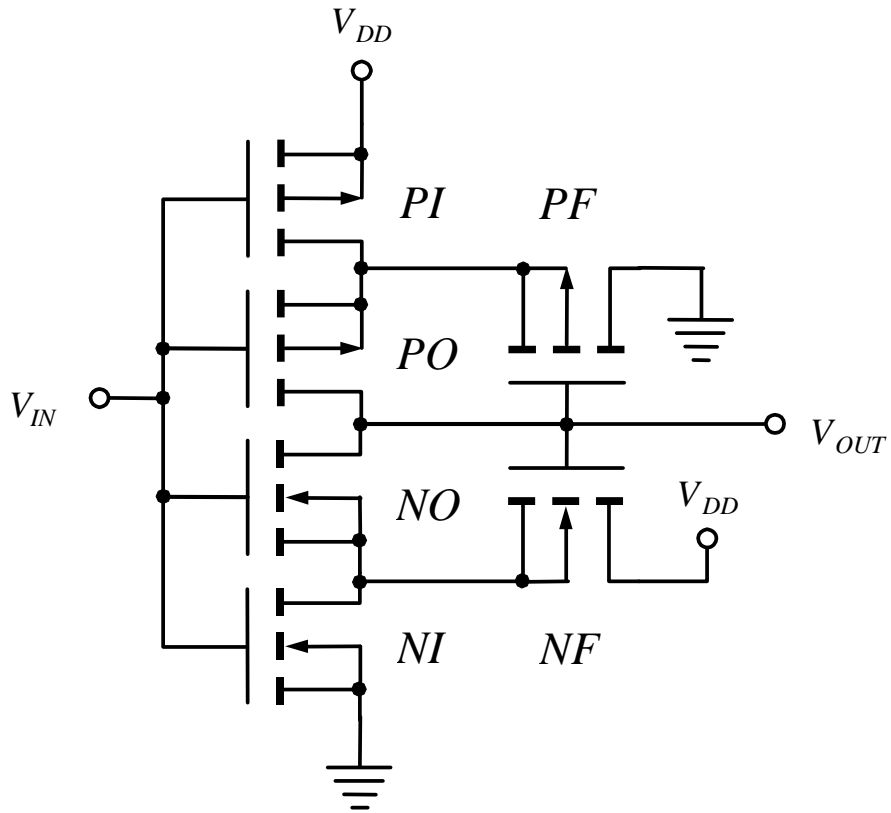


Fig. 2

3 (a) Find the minimum sum-of-products (SOP) expression for the following function using the Quine McClusky tabular method:

$$T = \Sigma (0, 2, 16, 18, 24, 26, 28, 30) \quad [40\%]$$

(b) Fig. 3 shows a combinational logic circuit. Assume that C and \bar{C} change at the same instant, as they are available from a bistable, and that the gates G1, G3 and G5 have each a delay of δ . G2 and G4 have larger delays of 2δ and 4δ respectively.

(i) Draw a clear timing diagram showing C changing from 0 to 1 with A=B=1. Demonstrate that there is a hazard, give its type and find the total delay before the output settles. [30%]

(ii) Redesign the circuit to remove the hazard, show its implementation using a selection of gates G1 to G5 and optimise the circuit for minimal total delay when C changes from 0 to 1 with A=B=1. Draw a timing diagram showing no hazard for this situation. [20%]

(iii) Re-optimize the circuit for minimal delay if any of A, B, C variables change, one at a time. What is the maximum delay in this case? [10%]

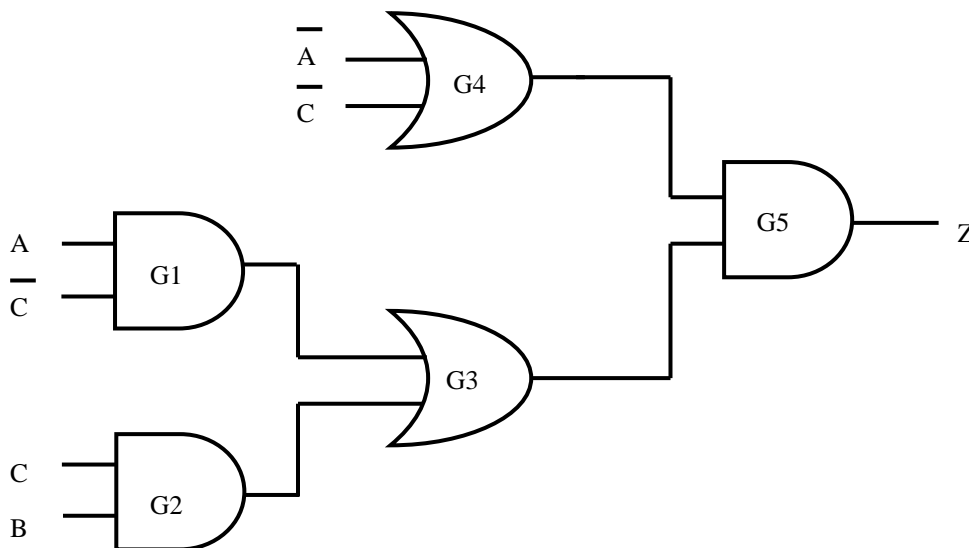


Fig. 3

4 A macro-cell, part of a complex combinational/sequential Programmable Array Logic (*PAL*) has been programmed as shown in Fig. 4. The binary gate signals on the *n-channel* MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1, B2 and B3. There are two main inputs labelled X and Y and one output labelled O1. The I/O2 pin can be configured either as an extra input or the second output of the macro-cell. The bistable is of *JK* type.

- (a) Describe the multiple operation of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [40%]
- (b) Derive the state diagram if the macro-cell is operated as a state-machine. Of what type of architecture is the state-machine? [30%]
- (c) Consider that the macro-cell is operated as a state-machine and only output O1 is of interest. Draw a simplified block diagram of the circuit. What specific function does the circuit perform? [30%]

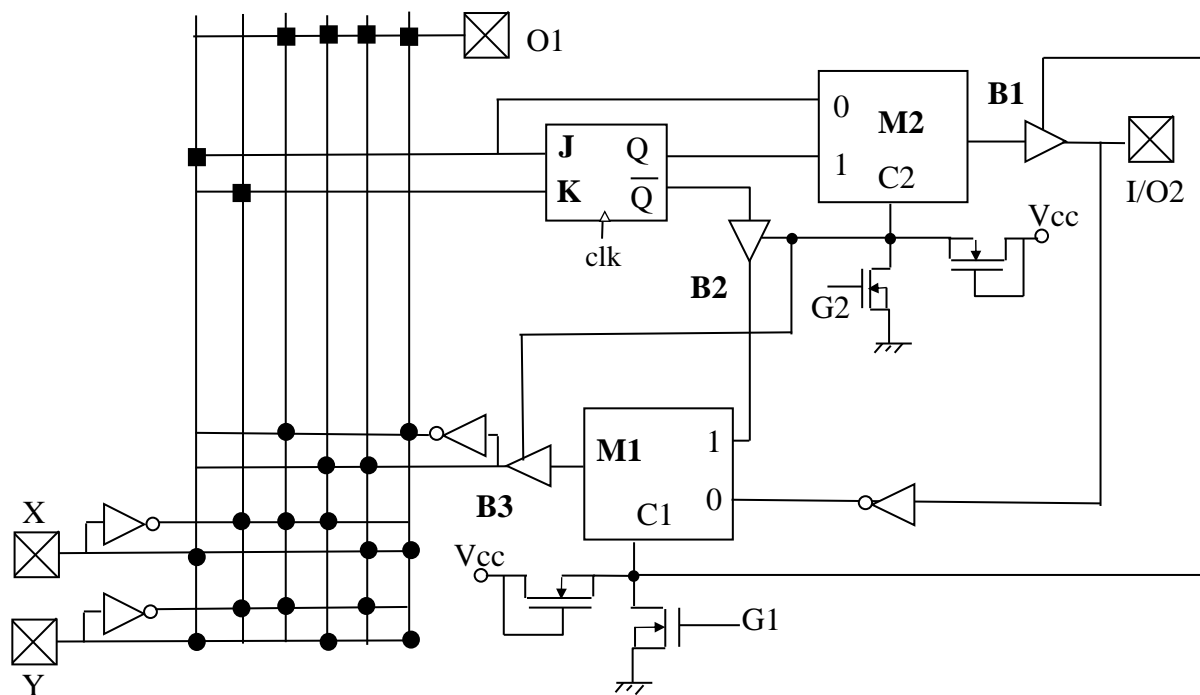


Fig. 4

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1(c)

For the n-type,

$$k_n = \frac{k'_n W}{L} = \frac{8 \times 8}{1+1} = 32 \mu\text{A/V}^2$$

For the p-type, $k_p = \frac{k'_p W}{L} = \frac{(4+4) \times 4}{1} = 32 \mu\text{A/V}$

By symmetry, $V_{\text{out}} = V_{\text{DS}} = V_{\text{DD}}/2 = 1.5 \text{ V}$,

Thus $I_D = \frac{k_n}{2} (V_{\text{GS}} - V_T)^2 = \frac{32}{2} (1.5 - 0.5)^2 = 16 \mu\text{A}$

3 (a) Final expression is $T = B' C' E' + A B E'$

(b) (i) dynamic hazard settling down after 5δ .

(ii) The minimal delay in the output when C changes from 0 to 1 for $A=B=1$ can be obtained as 2δ .

(iii) For better overall speed (when A and B also change, swap G2 and G5 giving a total delay of 3δ)

4 (a)

• If $G_1 = 1 \Rightarrow C_1 = 0$

○ $G_2 = 1 \Rightarrow C_2 = 0$

$$O_1 = \overline{X}\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1$$

○ $G_2 = 1 \Rightarrow C_2 = 1$

$$O_1 = \overline{X}\overline{Y}I + \overline{X}IY + \overline{I}YX + XYI = X \oplus Y \oplus I$$

• If $G_1 = 0$ and $G_2 = 1 \Rightarrow C_1 = 1, C_2 = 0$

$$\left\{ \begin{array}{l} O_1 = \overline{X}\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1 \\ O_2 = XY \end{array} \right.$$

• If $G_1 = 0$ and $G_2 = 0 \Rightarrow C_1 = 1, C_2 = 1$

The cell behaves as a MEALY sequential circuit. The inputs to the bistable JK are:

$$J = XY$$

$$K = \overline{X}\overline{Y}$$

$$O1 = X \oplus Y \oplus Q$$