EGT2
ENGINEERING TRIPOS PART IIA

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Friday 28 April 2017   9.30 to 11

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Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1   (a)   In a simple CMOS inverter, the n-channel MOSFET has threshold voltage V_{TN}, process transconductance k'_N and channel dimensions W_N and L_N. The corresponding parameters for the p-channel MOSFET are V_{TP}, k'_P, W_P and L_P. The power supply voltage is V_{DD}.

(i)   Derive an expression for the inverter *switching point voltage* V_{SP}, at which the output voltage and the input voltage are equal. Hence sketch a typical transfer characteristic, clearly showing the switching point V_{SP}.   [30%]

(ii)   Briefly discuss the measures that must be taken in the design of an inverter to position V_{SP} midway between the supply rails. What are the advantages and disadvantages of doing so?   [20%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad\qquad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance.

(b)   Figure 1 shows the organisation of a simple static random-access memory cell. Explain briefly the mode of operation of this circuit, and describe the role of the signals *word* , *bit* , and $\overline{bit}$ in allowing data to be written and read.   [25%]

(i)   What special measures need to be taken in the design of the inverters A and B to allow the circuit to work correctly?   [10%]

(ii)   Describe in outline the additional circuit elements necessary to allow the cell to be interfaced to an external circuit.   [15%]
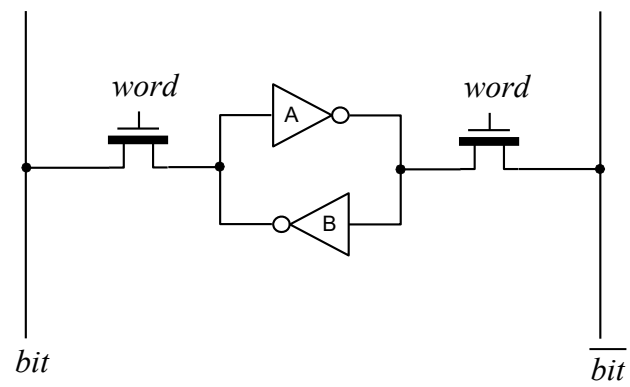
Fig. 1

(TURN OVER

2   (a)   Give the reasons for the popularity of CMOS technology in the design of digital logic systems. What are the disadvantages of CMOS? Your answer may include references to: implementation, compactness, input and output levels, and drive capability, as well as any other factors you consider important.   [30%]

(b)   With the aid of a diagram, show how to determine the noise margins from the input and output logic levels V_{IL}, V_{IH}, V_{OL} and V_{OH}.   [20%]

(c)   Characteristics of inverter gates taken from a certain manufacturer's CMOS and bipolar logic catalogue are given in simplified form in the Table below. All data correspond to operation using a 10 V supply. The tabulated information shows input and output logic levels as well as the maximum gate input currents in the high and low states. A negative input current signifies a current which flows out from the gate's input terminal.

	V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{IHmax}	I_{ILmax}
Bipolar logic	0.8 V	2.0 V	0.4 V	7.4 V	40 μA	−1.6 mA
CMOS logic	1.0 V	8.5 V	0.1 V	9.9 V	0	0

Determine the noise margins that will apply when:

   (i)   a bipolar inverter drives a single CMOS inverter;

   (ii)   a CMOS inverter drives a single bipolar inverter.

Comment on these results.   [30%]

(d)   How would you expect the noise margins to be affected in each case, in part (c), if twenty inputs were driven instead of one? State any assumptions made.   [20%]

3   (a)   Explain the differences between *Mealy* and *Moore* sequential circuits.   [10%]

(b)   Figure 2 shows the implementation of a sequential circuit. Is this a Mealy or a Moore configuration? Explain your answer.   [20%]

(c)   The circuit of a 2-bit comparator is shown in Fig. 3. It compares two binary numbers, *A* and *B*, each of two bits, and produces their relation such that one number is less than, or equal to, or greater than the other.

    (i)   Build the truth table and find the output functions.   [30%]

    (ii)   Implement the output functions using either a ROM or a PLA. Comment on your choice.   [20%]

(d)   Using only 2-bit comparator circuits, as shown in Fig. 3, implement a 4-bit comparator circuit.   [20%]
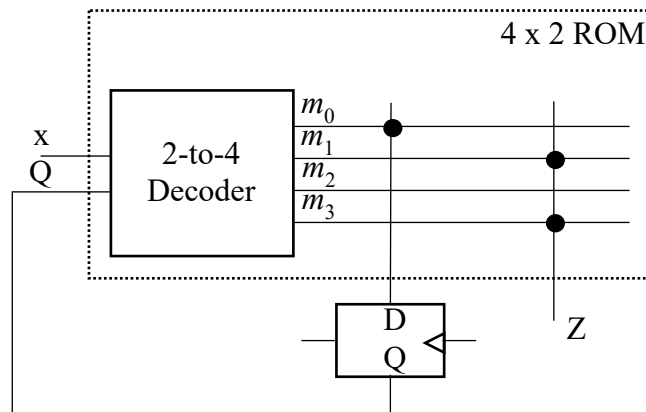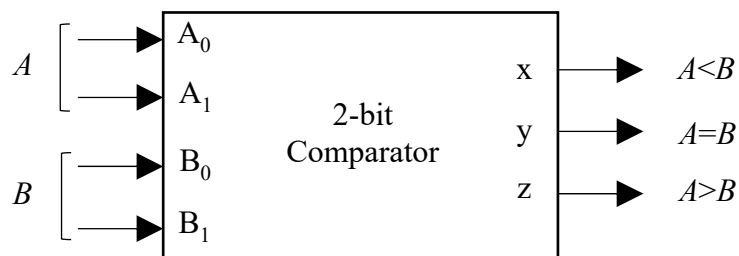

Fig. 2

Fig. 3

4   (a)   Briefly discuss the advantages and disadvantages of implementing logic functions with *multiplexers*, *ROMs*, and *PLAs*.   [20%]

(b)   In order to automate its storage facilities, a warehouse has decided to design the sorting conveyor system shown in Fig. 4. The sorter controller can detect the length of incoming boxes (to be stored) and divert only the ones that are long. For simplicity, you may assume that all boxes are of only two sizes, either small or big. Using two sensors (S_1 and S_2), the small boxes will never pass under both sensors at one time, however, the big ones will. The sensor input will be set to logic high when a box is under the sensor, otherwise it will remain at zero. After a big box is detected (i.e. the end of the box passes sensor S_2), the sorter must be activated, which will divert the box to the second output. You may also assume that there will always be sufficient space between boxes such that two will never be under the sensors at the same time.

For all input sequences that are not physically possible, ensure that your system returns to the initial state. Furthermore, all unused states should return your system to the initial state.

   (i)   Design the sorter controller shown in Fig. 4. Draw the state diagram and the state table.   [40%]

   (ii)   Draw the circuit implementation of the controller using J-K bistables and logic gates.   [20%]

   (iii) Comment on the existence of hazards, if any, in the implemented circuit.   [20%]
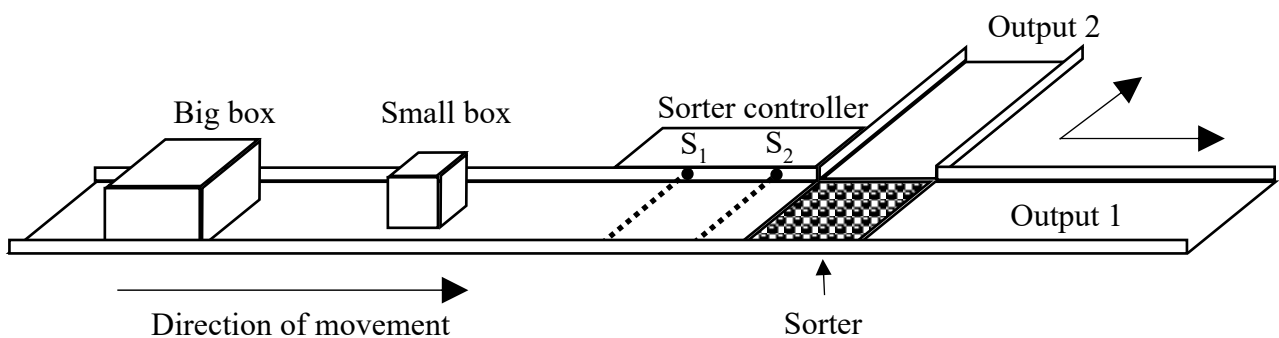

Fig. 4

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