Version PRP/5

EGT2
ENGINEERING TRIPOS PART IIA

Monday 25 April 2016 9.30 to 11

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) A switched mode dc-dc power supply chip is designed to provide power for smart controls on domestic appliances. The ac mains input circuits recommended are shown in Fig. 1 (a) for 0.25-1 W and Fig. 1(b) for 1-10 W. The resistors RF1 are fuses and may be neglected.

(i) For Fig. 1 (a) state the type of rectifier circuit and comment on the use of two diodes. [10%]

(ii) Explain carefully why the circuit of Fig. 1 (b) is recommended for power levels above 1 W. [15%]

(iii) Noting that the circuit in Fig. 1 (b) forms the supply to the switched mode power supply chip, give two reasons for splitting the smoothing capacitance into C_{IN1} and C_{IN2} with a small value inductor separating them. [10%]

(iv) The application note recommends the following equation to calculate the total smoothing capacitance C_{IN}, where $V_{\min}$ is the minimum smoothing capacitor voltage, P_O and η are the output power from the power supply and its efficiency, t_c is the conduction time of the diodes and V is the ac mains voltage with frequency f. Stating your assumptions, show how the following equation is obtained. [20%]

$$C_{IN}\frac{V_{\min}^2}{2} = C_{IN}V^2 - \frac{P_O}{\eta}\left(\frac{1}{2f} - t_c\right)$$

(b) A power factor controller based on ultra fast IGBTs is shown in Fig. 2. V is 230 V, and the dc output voltage is 400 V with a constant load current of 6.25 A.

(i) Describe briefly the operation of the circuit during a positive half cycle of V, noting the sequence of conduction of the pairs of devices for a few cycles of the modulation applied to S_1 and S_2. [15%]

(ii) Comment on the types of diode needed for D_1, D_2 and D_3, D_4. [10%]

(iii) Sketch the voltage across the capacitor C_o for a few cycles of the ac supply and estimate the voltage ripple on the capacitor C_o, if its capacitance is 0.22 mF. [20%]

(Hint: Fourier Series are given in the Maths Databook)

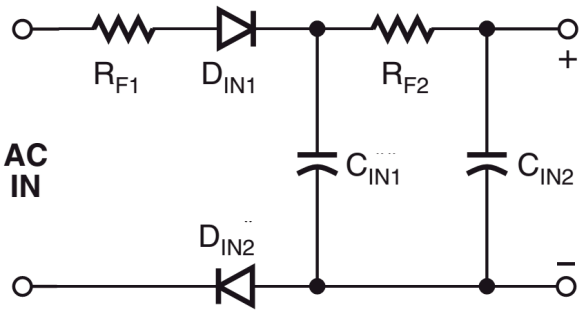

Fig. 1(a)

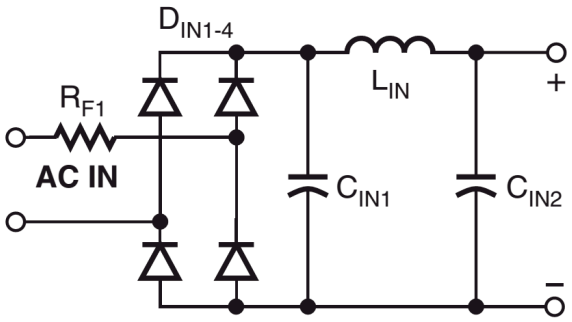

Fig. 1(b)

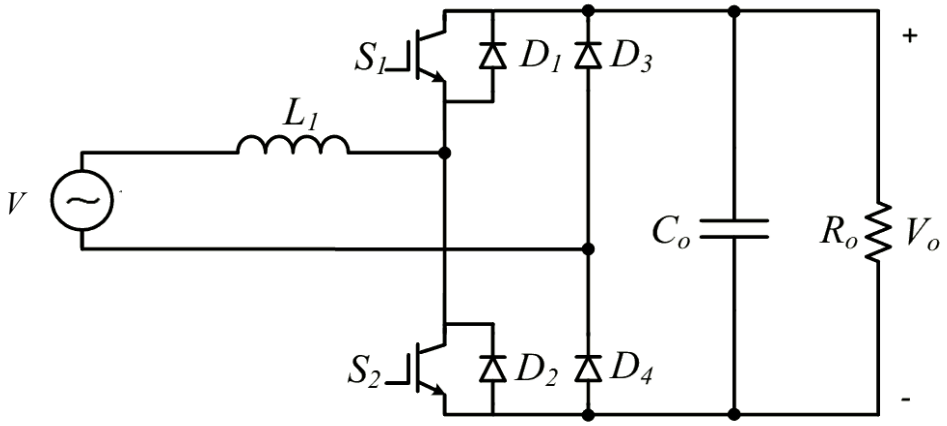

Fig. 2

2 (a) Explain why a base current is required in a Bipolar Junction Transistor (BJT) during its on-state in a switching circuit. [10%]

(b) Carefully sketch a cross section of a typical Insulated Gate Bipolar Transistor (IGBT) structure and explain how the base current is provided to the constituent BJT within the IGBT structure. [20%]

(c) Figure 3 shows the waveforms of a BJT switch in a switching circuit with an inductive load. The switch operates at a switching frequency $f = 40$ kHz with a duty cycle $D = 50\%$. The other parameters are: line voltage $V_{dc} = 300$ V, on-state collector current $I_C = 1.5$ A, on-state base current $I_B = 0.3$ A, collector-emitter on-state voltage $V_{CE} = 2$ V, base-emitter on-state voltage drop $V_{BE} = 1$ V.

(i) Sketch the path across the forward characteristics for turn off and turn on. [15%]

(ii) Estimate the switching and total power losses in the BJT. [30%]

(iii) It is suggested that a 0.02 μF capacitor is connected across the collector-emitter terminals of the BJT. Assuming that the current falls at the same rate as previously, and the collector-emitter voltage rise is controlled by the capacitor, find the collector-emitter voltage at the end of the current fall and sketch the current and voltage waveforms versus time for one turn off. [15%]

(iv) State the mode in which the circuit of part (iii) must be operated and why. [10%]

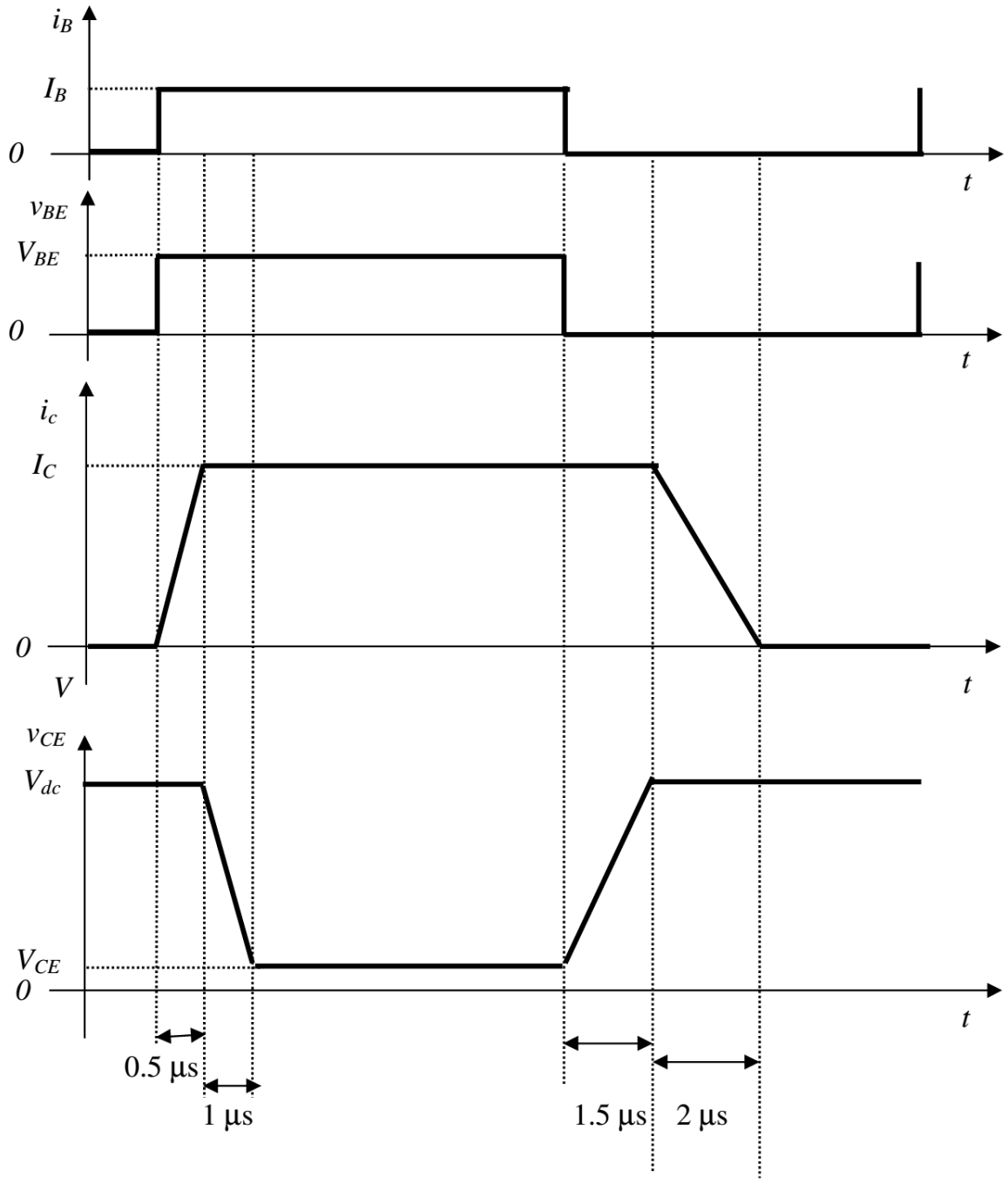

Fig. 3

3 Figure 4 shows a step-down dc-dc converter circuit based on the LinkSwitch-TN integrated converter for a specific low cost, low power load. A design choice arises between continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

(i) With reference to sketches of the inductor current waveform, explain carefully the meaning of the terms CCM and DCM and create a table comparing the influence of the conduction mode on the efficiency and the ratings of the four main components: the MOSFET in the LinkSwitch-TN, D, L and C. [35%]

(ii) Give two reasons why the non-isolated step-down topology is preferred over other topologies for such applications. [10%]

(iii) For a step down from 325 V to 15 V, sketch the LinkSwitch-TN MOSFET current when operating in DCM. [15%]

(iv) If the converter operates on the boundary of DCM and CCM, with a peak current of I_{pk}, then find the RMS current in the inductor as a ratio of I_{pk} and hence discuss carefully the efficiency of the converter. [25%]

(v) The controller principle in the LinkSwitch-TN is based on *cycle skipping*, independent of the mode of operation. Cycle skipping refers to dropping whole pulses of on time when the voltage at the output is above the reference level chosen. Find the duty cycle it will operate at under the conditions stated above and hence suggest two reasons why cycle skipping is a good principle for operating such a converter. [15%]

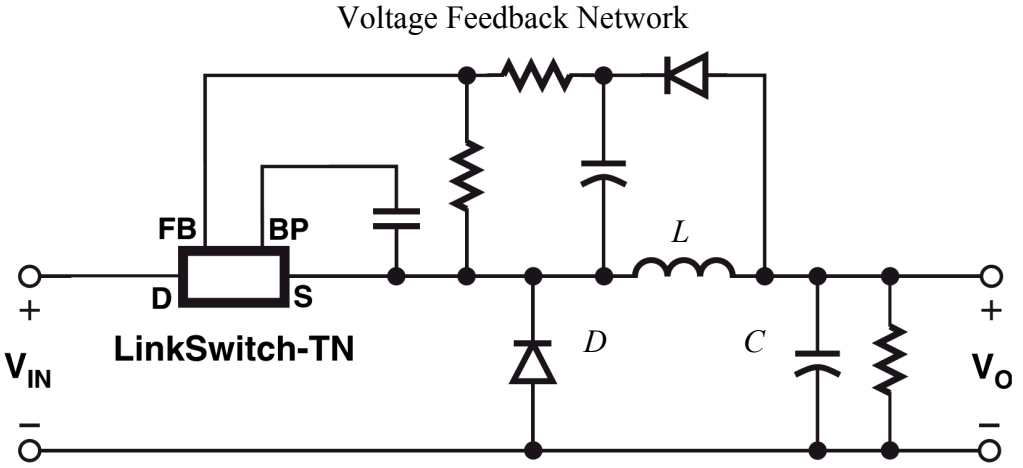

Fig. 4

4 (a) The voltage outputs from a PWM inverter illustrated in Fig. 5, are sometimes described as *two level*. Making reference to the duty ratio *D*, explain why this is a clear description when the inverter leg is converting the dc supply voltage to an ac voltage. Describe carefully one method by which the switching signals for T1 and T4 may be obtained. [20%]

(b) A three phase bridge inverter operates in conventional sinusoidal PWM mode.

(i) Explain why there is no third harmonic or other thirds appearing in the line-to-line load voltage. [10%]

(ii) Show that adding a value of 1/6, relative to the fundamental, of the third harmonic to the desired sinewave phase voltage output will give the maximum distortion free load voltage from sine PWM. [20%]

(iii) Find the new maximum distortion-free load voltage as a percentage of the dc supply voltage. [10%]

(c) Space Vector Modulation is a method of producing the modulation signals for the whole inverter of Fig. 5 based on the position of a single *voltage vector*.

(i) Describe briefly the *Direct-Inverse* sequence by which the operation of the inverter may be optimised for low switching losses. [10%]

(ii) Consider a vector of magnitude 0.5×0.866 relative to the magnitudes of the vector **A** (1,0,0) and at an angle of 30° to **A**. Find the duty ratios for V_a, V_b and V_c optimised for low switching losses. Hence or otherwise show that the switching losses may be minimised at this vector position by adding a particular dc component to the voltage produced at each inverter output. [30%]

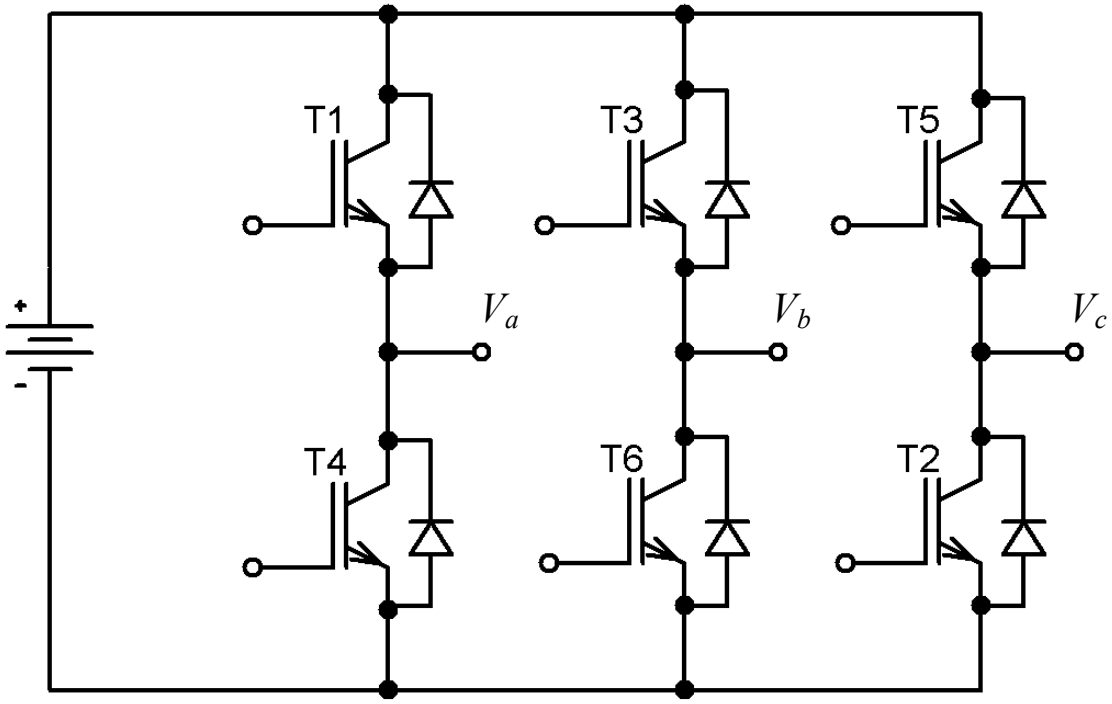

Fig. 5

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