Version SH/3

EGT2
ENGINEERING TRIPOS PART IIA

Thursday 30 April 2015 9.30 to 11

Module 3B5

SEMICONDUCTOR ENGINEERING

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 An electron with an energy E exists in a one-dimensional potential well of the form

$$V(x) = \begin{cases} 0 & \text{for } x < 0 \ (\text{region I}) \\ V_0 & \text{for } x \geq 0 \ (\text{region II}) \end{cases}$$

For the situation where $V_0 > E$, the solution to the *Time-Independent Schrödinger Equation* (TISE) is a wavefunction of the form

$$\psi(x) = \begin{cases} A\exp(-jk_I x) + B\exp(jk_I x) & \text{for } x < 0 \ (\text{region I}) \\ C\exp(-k_{II} x) + D\exp(k_{II} x) & \text{for } x \geq 0 \ (\text{region II}) \end{cases}$$

where *A*, *B*, *C* and *D* are constants.

(a) Why must $D = 0$? [10%]

(b) Find expressions for each of *B* and *C* in terms of *A*. [30%]

(c) Why must $|A| = |B|$? [10%]

(d) If $V_0 = 1\,\text{eV}$ and $E = 0.62\,\text{eV}$, for what value of x will the probability of the electron existing at a particular location in region II have decreased by factor of $\exp(-1)$ compared with the probability of the electron being at $x = 0$? [30%]

(e) Explain why scaling down the physical dimensions of a *Metal Oxide Semiconductor Field Effect Transistor* (MOSFET) leads to problems with gate leakage. How may this be mitigated? [20%]

NOTE: The TISE in one dimension is

$$\frac{-\hbar^2}{2m}\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} + V\psi = E\psi$$

2 (a) (i) Why must electrons exist in certain, well-defined energy levels in single atoms? What experimental evidence is there for this? [15%]

(ii) The electronic configuration of lithium, which has an atomic number of 3, is $1s^2\ 2s^1$. What is the electronic configuration of silicon, which has an atomic number of 14? [10%]

(iii) Why do electrons exist in bands of energy states in a solid? Hence explain why silicon behaves as a semiconductor. [20%]

(b) For the Nearly Free Electron Theory, the density of electron states in a solid of volume V is given by

$$g(E)dE = \frac{V}{2\pi^2\hbar^3}\left(2m^*\right)^{3/2} E^{1/2}dE$$

where m^* is the *effective mass* of the electrons. The Fermi function is

$$f(E) = \frac{1}{\exp\left(\dfrac{E - E_F}{kT}\right) + 1}$$

(i) Show that the number density of free electrons in the conduction band of a solid is

$$n = N_C \exp\left(\frac{E_F - E_C}{kT}\right)$$

and calculate the value of N_C for silicon at 298 K where the effective mass of electrons in the conduction band is $1.09m_e$, and m_e is the free electron mass. [30%]

(ii) Estimate the impurity concentration required to dope silicon n-type so that $E_C - E_F = 0.1\,\text{eV}$. State all assumptions made. [15%]

(iii) What limits the maximum built-in potential that can be achieved across a *pn junction* made using silicon on both sides of the junction? [10%]

NOTE: $$\int_0^\infty x^2 \exp\left(-\alpha x^2\right)dx = \frac{1}{4}\sqrt{\frac{\pi}{\alpha^3}}$$

3 (a) For a *p-channel enhancement Metal Oxide Semiconductor Field Effect Transistor* (MOSFET), sketch the output and transfer characteristics (i.e. how the drain-source current varies with drain-source voltage and gate-source voltage, respectively). Explain features of the characteristics using the terms *threshold voltage* and *pinch-off*. [15%]

(b) An ideal MOS capacitor is formed on an n-type Si substrate with a doping density of $N_D = 10^{22}$ m^{-3}. The SiO_2 thickness is 20 nm and its relative permittivity is 3.9. The intrinsic carrier concentration of silicon is 1.5×10^{16} m^{-3}. Assume room temperature (298 K) operation.

(i) Draw a band diagram for the MOS capacitor at the point of strong inversion. In the band diagram, show clearly the externally applied bias, the voltage drop across the n-type Si and the position of the Fermi level with respect to an intrinsic level that lies midgap. [10%]

(ii) The potential V_s at the Si-SiO_2 interface relates to the width w of the Si depletion region via

$$V_s = \frac{eN_D w^2}{2\varepsilon_o \varepsilon_r}$$

where ε_o is the permittivity of free space and $\varepsilon_r = 12$ the relative permittivity of Si. Show that the maximum width of the depletion region in the Si, which occurs at the point of strong inversion, is approximately 300 nm. [25%]

(iii) Explain at which bias voltage the MOS structure shows the lowest capacitance. Calculate this minimum capacitance per unit area. State all assumptions made. [25%]

(iv) The MOS capacitor is used to fabricate an enhancement MOSFET. Explain what is meant by *sub-threshold conduction* and its importance for transistor switching. [10%]

(c) On the basis of MOS device operation, explain the principle of flash memory. [15%]

4 (a) An abrupt *pn junction* is fabricated from crystalline silicon. The concentration of acceptors in the p region is $N_A = 10^{24}$ m^{-3}, and the concentration of donors in the n-region is $N_D = 10^{21}$ m^{-3}. Assume room temperature (298 K) operation. The intrinsic carrier concentration of silicon is 1.5×10^{16} m^{-3}.

(i) Calculate the Fermi level positions in the p and n regions. [10%]

(ii) Draw an equilibrium band diagram for the junction and determine the built in potential from the diagram. [10%]

(iii) Sketch the electric field across the unbiased junction. Starting from the Poisson equation, derive an expression for the maximum electric field in the junction. [25%]

(b) A p^+n junction and np junction are combined so they share the n-type region. The p^+n junction is forward biased and the np junction is reverse biased. W is the undepleted width of the n-type region and L_h is the diffusion length of holes in the n-type region.

(i) Sketch the distribution of holes across the shared n-type region assuming that the diodes are not coupled, i.e. $W >> L_h$. [10%]

(ii) Sketch the distribution of holes across the shared n-type region for $W << L_h$.

[10%]

(iii) Outline the basic principle of a *bipolar junction transistor* (BJT), in particular how amplification can be achieved. Explain why the base-to-collector current amplification factor β can be approximated as

$$\beta \approx \frac{\tau_{base}}{\tau_{transit}}$$

where τ_{base} is the minority carrier lifetime in the base, and $\tau_{transit}$ the average transit time of minority carriers across the base. [20%]

(c) A *Shockley diode* is a two-terminal device that consists of three pn diodes, J1, J2 and J3, in series. Draw a band diagram for such a pnpn device in the so-called *forward-off state,* where most of the externally applied voltage drops across J2 which is reverse biased, whereas J1 and J3 are forward biased. [15%]

END OF PAPER

Numerical Answers:

Q1(d) x=0.158nm; Q2(b)(i) Nc=2.825×10^{25} m^{-3}, (b)(ii) N_D=5.76×10^{23} m^{-3}; Q3(b)(iv) C_{min}= 2.9×10^{-4} F/m^2; Q4 (a) (i) n-region: E_F-E_i=0.28eV, p-region: E_i-E_F=0.46eV, (ii) eV_0=0.74 eV