Version AHG/3

EGT2
ENGINEERING TRIPOS PART IIA

Tuesday 19 April 2016 9.30 to 11

Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Explain why the latency of the arithmetic logic unit (ALU) is of paramount importance in computer hardware design. [10%]

(b) Describe the operation of a single level, 4-bit carry-lookahead adder. How many gate delays are required to produce the sums and the carry-out from the fourth bit? [25%]

(c) Figure 1 shows an alternative design of a 4-bit adder. There are two 2-bit adders connected together using ripple-carry. Each 2-bit adder uses one level of carry-lookahead to calculate the internal carry, and a second level of carry-lookahead to calculate the carry-out from the most significant bit.

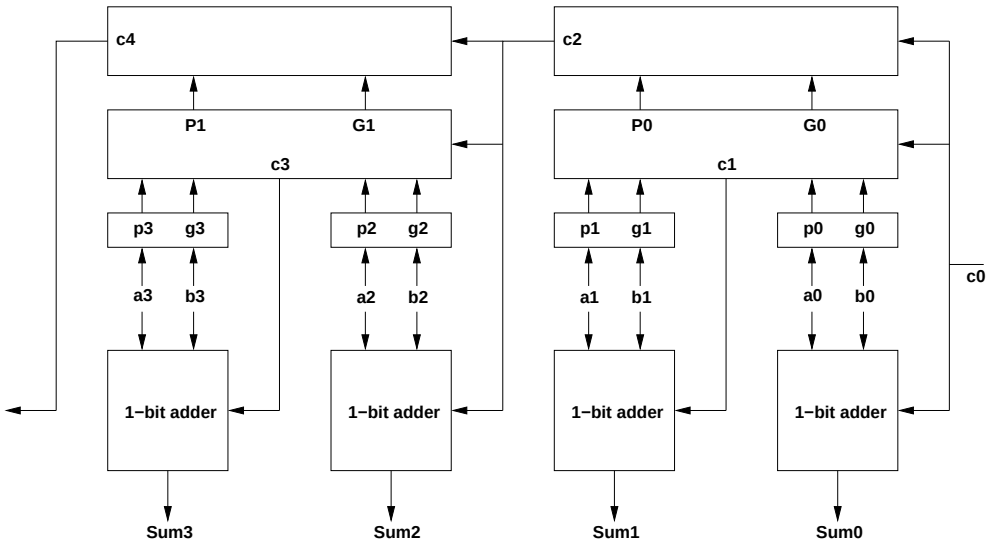

Fig. 1

Write down expressions for:

(i) p1 and g1 in terms of a1 and b1; [5%]

(ii) P0 and G0 in terms of p0, p1, g0 and g1; [10%]

(iii) c2 in terms of P0, G0 and c0; [5%]

(iv) c3 and c4 in terms of c2 and other signals. [15%]

How many gate delays are required to produce the sums and c4? [10%]

(d) Discuss the relative advantages and disadvantages of the designs in (b) and (c). [20%]

2 (a) Explain why the inclusion of a cache, between the CPU and main memory, generally improves a computer's performance. [15%]

(b) Discuss briefly the relative advantages and disadvantages of direct mapped and set-associative caches. [20%]

(c) What requirements of a modern computer system motivate the adoption of a virtual memory system? [15%]

(d) A certain computer has a byte-addressable memory with 4-byte words. Both the virtual and physical addresses are 32 bits wide and the page size is 4 KBytes. The translation lookaside buffer (TLB) is fully associative with 64 rows and a block size of two page table entries (i.e. the TLB stores 128 page table entries). The 64 KByte data cache is direct-mapped, with a block size of four words. Sketch a hardware schematic showing the entire process of retrieving a data word, starting from the virtual address. Include details of how the virtual and physical addresses are split into page numbers and page offsets, and any cache/TLB tags, indices and offsets. Assume hits at both the TLB and cache levels, so there is no need to show the page table or the main memory system. [50%]

3 (a) What is the main purpose of the Open Systems Interconnect (OSI) reference model? Identify three key properties that the model must exhibit in order to achieve this goal. Sketch the OSI model, including the different environments, for two computers interconnected via a network. [40%]

(b) The lowest layer in the OSI reference model allows two computers to be connected physically. Explain how this layer can be modified to allow non-OSI compliant or proprietary services within the communications system. [30%]

(c) The Asynchronous Transfer Mode (ATM) protocol was designed to be compatible with the Integrated Services Digital Network (ISDN) as part of the Synchronous Digital Hierarchy (SDH). Explain briefly the defining features of the ATM protocol and discuss its compatibility with the OSI reference model. [30%]

4 (a) An Asymmetric Digital Subscriber Line (ADSL) modem is a key piece of technology underpinning the expansion of broadband networks in the home. Describe the basic operation of an ADSL modem and explain why it performs much better than older, dial-up modems. Why do the asymmetry and the distance from the local exchange both affect the total achievable bandwidth? [40%]

(b) The majority of modern ADSL connections run using Ethernet and the Internet Protocol (IP) in tandem with the Transmission Control Protocol (TCP). Sketch a simple diagram to show how these three protocols are combined in such a connection. Describe the key functions of each protocol in terms of overall network operation. How do these protocols relate to the Open Systems Interconnect (OSI) reference model? [35%]

(c) Explain why the combination of protocols in (b) is used in this way. Do you think this represents the most effective use of the bandwidth available from an ADSL connection? How might a network be redesigned to use the ADSL bandwidth more efficiently? What would be the main penalty for this change? [25%]

END OF PAPER

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Numerical Answers

1. (c) 5 gate delays
   (d) 9 gate delays