Version AN/2

EGT3
ENGINEERING TRIPOS PART IIB

Monday 20 April 2015 2 to 3.30

Module 4B21

ANALOGUE INTEGRATED CIRCUITS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Attachment: 4B21 Analogue Integrated Circuits data sheet (2 pages).
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) With the aid of one of more circuit schematics, describe the operating principle of a current mirror. State one application of the current mirror in an amplifier circuit. [25%]

(b) The circuit shown in Fig. 1 is an integrated MOS current mirror. The transistors in the circuit have the following parameters: $(W/L)_{Q1} = 50\mu m/5\mu m$, $|V_{A2}| = |V_{A1}| = 200$ V, $V_t = 1$ V, $\mu_n \cdot C_{ox} = 20\ \mu A \cdot V^{-2}$ and with a reference current of 100 μA. Assuming that there are no channel length modulation effects:

(i) what is the value of V_{GS}, [10%]

(ii) what is the lowest possible value of V_o for the mirror to supply a constant current output, [10%]

(iii) show that, if $V_o = V_{GS}$, then $\frac{I_o}{I_{REF}} = \frac{(W/L)_{Q2}}{(W/L)_{Q1}}$, [15%]

(iv) what is the output resistance of the current mirror at $I_o = 100\ \mu A$. [15%]

(c) If the output voltage increases by 20% from its value in part (iii) at $I_o = 100\ \mu A$, what will be the corresponding change in output current? Discuss the physical implications of your result. [25%]

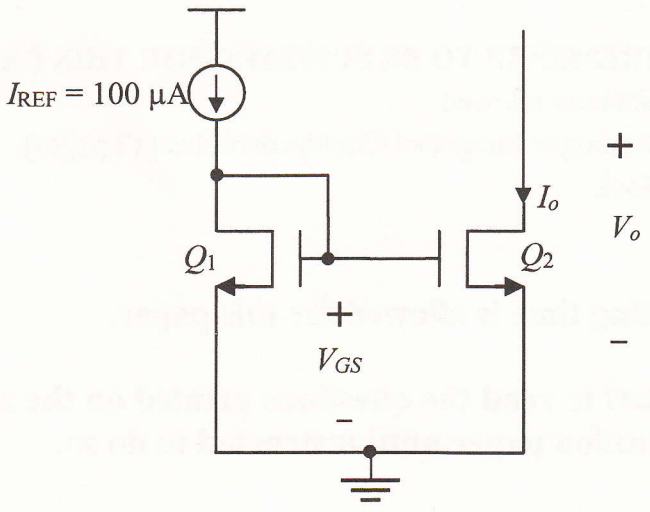

Fig. 1

2 (a) What is a multi-stage amplifier? [10%]

(b) Explain why multistage amplifiers are necessary from the standpoint of circuit characteristics. [10%]

(c) The two-stage CMOS op-amp in Fig. 2 is fabricated in a 0.18 μm technology having $k_n' = 4k_p' = 400\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.4$ V. With A and B grounded, perform a DC design that will result in each of Q1, Q2, Q3 and Q4 conducting a drain current of 200 μA. Design so that all transistors operate at 0.2 V overdrive voltage. Assume that the current through Q6 and Q7 is $2I_{REF}$.

(i) Specify the W/L ratio in tabular form required for each MOSFET. [15%]

(ii) What is the DC voltage at the output ideally? [15%]

(iii) Calculate the input common mode range. [15%]

(iv) Find the allowable range of the output voltage. [15%]

(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 5V. [20%]

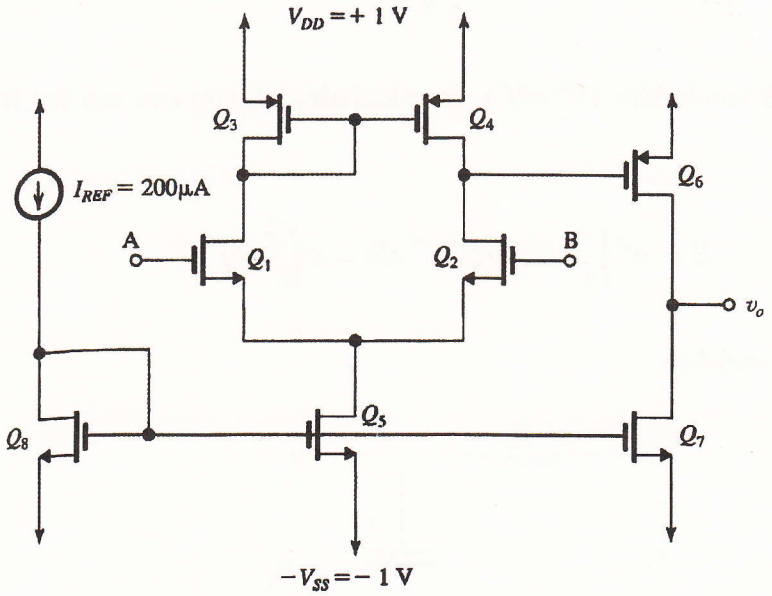

Fig. 2

3 (a) Name three sources of noise that are commonly found in integrated circuit components. [20%]

(b) What is meant by the noise figure of an amplifier and describe how you would measure it. [30%]

(c) A parallel combination of identical resistors are connected between the input and ground terminals of a low noise amplifier. The output of the amplifier has a flat spectrum with value –100 dB/Hz. If the voltage gain of the amplifier is 1000, calculate the resistor values. In your calculations, assume that the amplifier is ideal (i.e., noiseless). [20%]

(d) A filter or network has an equivalent noise bandwidth B, which can be stated as:

$$B = \frac{1}{|A_o|^2}\int_0^\infty |A(f)|^2\, df$$

where A_o denotes the transmission (voltage or current) magnitude, $A(f)$ the transfer function, and f the frequency. The above equation yields the same results as the actual non-ideal bandwidth the filter or network has in practice.

For the single-pole filter shown in Fig. 3, show that the noise equivalent bandwidth B is

$$B = \frac{\pi}{2} f_o$$

where f_o is the -3 dB bandwidth $1/(2\pi RC)$. In calculating B, you can use the following relation,

$$B = a^2\int_0^\infty (a^2+b^2)^{-1}\, db = a\int_0^{\frac{\pi}{2}} dq$$

where q is a dummy variable. [30%]

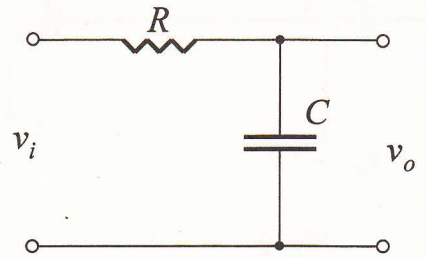

Fig. 3

4 (a) Explain how the design principle of the current-steering circuit differs from that of a current mirror. [30%]

(b) The current-steering circuit shown in Fig. 4 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 80\ \mu A/V^2$, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, and the Early voltages are $V_{An}' = 10$ V/μm, $|V_{Ap}'| = |12|$ V/μm. If the channel length L of all devices is 0.8 μm, design the circuit so that $I_{REF} = 20\ \mu A$, $I_2 = 100\ \mu A$, $I_3 = I_4 = 20\ \mu A$ and $I_5 = 50\ \mu A$. Use minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as +1.3V and proper operation of the current sink Q_5 with voltages at its drain as low as -1.3V.

(i) Specify the widths of all devices and the value of R. [40%]

(ii) Find the output resistance of the current source Q_2. [15%]

(iii) Find the output resistance of the current sink Q_5. [15%]

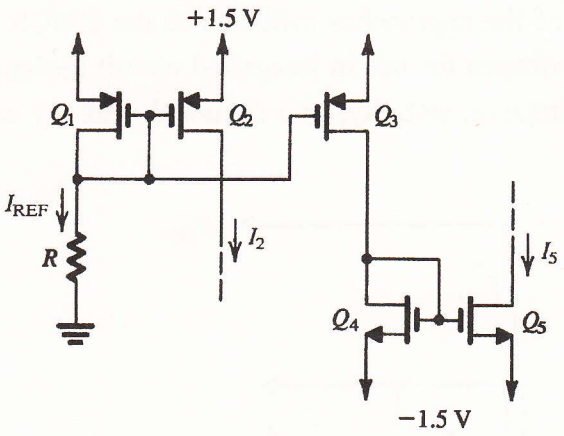

Fig. 4

5 Consider the circuit of Fig. 5, in which an NMOS transistor *M1* is connected in a circuit designed to provide a reference voltage V_{REF}.

(a) Derive an expression relating V_{REF} with the drain current I, the transistor parameters and other circuit constants. [20%]

(b) For transistor *M1*, the channel dimensions W and L are chosen as 40 μm and 4 μm, respectively, $V_t = +1$ V, and $k' = 20 \times 10^{-6}$ AV^{-2}. V_{DD} and V_{SS} are 6 V and 0 V respectively.

Deduce a suitable value for R if V_{REF} is to be 2 V, and determine the drain current I. [20%]

(c) What is meant by the following terms in the context of the performance of voltage references, and why are they important?

(i) Power supply sensitivity.

(ii) Fractional temperature coefficient. [20%]

(d) Write a short account of the approaches available to the CMOS IC designer for generating stable reference voltages for use in integrated circuit design. Your account should mention power consumption, stability, area occupied, and any other factors you consider to be important. [40%]

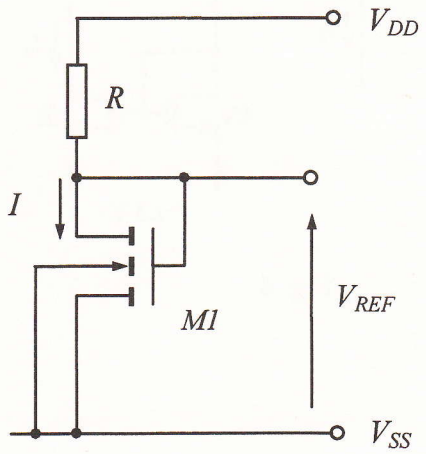

Fig. 5

END OF PAPER

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FORMULA SHEET

Bipolar Junction Transistors:

$$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$$

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$$

MOSFETs:

$$i_D = K[2(v_{GS} - V_t)v_{DS} - {v_{DS}}^2] \qquad K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$$

$$i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad k' = \mu C_{ox}$$

$$g_m = 2K(v_{GS} - V_t) \qquad r_O = \frac{|V_A|}{I_D}$$

Differential Amplifiers:

$$v_o = A_d v_d + A_{cm} v_{cm}$$

$$CMRR = 20\log|A_d / A_{cm}| \qquad A_{cm} = \frac{v_o}{v_{cm}} \qquad A_d = \frac{v_o}{v_d} = g_m R_D$$

OR OR

$$A_{cm} = \frac{\Delta R_D}{2R} \qquad A_d = \frac{\Sigma R_C}{\Sigma R_E}$$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2}$ $\qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = emitter\ resistance$$

FET small signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$ $\qquad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1-K)$ $\qquad K \equiv \frac{V_2}{V_1}$

Thermal Noise: $< {v_n}^2 >= 4kTBR$ $\qquad k = 1.38x10^{-23}\ J/K$

Feedback Architectures and Properties:

	Series-Shunt	**Series-Series**	**Shunt-Series**	**Shunt-Shunt**
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set[1]	$V_o=0$	$I_o=0$	$I_o=0$	$V_o=0$
To find output loop, set[1]	$I_i=0$	$I_i=0$	$V_i=0$	$V_i=0$
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_v = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1+\beta A$	$1+\beta A_v$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
A_f	A_v/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$R_o/(1+\beta A_v)$	$R_o(1+\beta G_M)$	$R_o(1+\beta A_i)$	$R_o/(1+\beta R_M)$
$R'_{of}=R_{of} \lVert R_L$	R'_o/D	$R'_o(1+\beta G_M)/D$	$R'_o(1+\beta A_i)/D$	R'_o/D

[1]This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L, and R_S into account.