Version AN/3

EGT3
ENGINEERING TRIPOS PART IIB

Friday, 29th April 2016 09:30-11:00

Module 4B21

ANALOGUE INTEGRATED CIRCUITS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Attachment: 4B21 Analogue Integrated Circuits Data Sheet (2 pages).
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) With the aid of one or more circuit schematics, describe the operating principle of a current mirror and how one would scale the output current. [20%]

(b) The circuit shown in Fig. 1 is to be designed using a 0.18 μm CMOS process. The transistors have the following parameters: $\mu_n \cdot C_{ox}$ = 387 μA·V^{-2}, $\mu_p \cdot C_{ox}$ = 86 μA·V^{-2}, $V_{tn} = -V_{tp}$ = 0.5 V, V_{DD} = 1.8 V, V'_{An} = 5 V/μm, and V'_{Ap} = –6 V/μm. The output voltage is to swing between 0.2 V to 1.6 V and the voltage gain must be at least 10 V/V.

(i) Using the same channel length of transistors, design the circuit for a bias current of 50 μA. [20%]

(ii) If the channel length is to be an integer multiple of 0.18 μm, what is its value? [15%]

(iii) What is the new value of channel length if the gain is to be increased by a factor of 2? [20%]

(iv) What is the resulting increase in total gate area? [15%]

(c) State one application of the current mirror in a multi-stage amplifier. [10%]

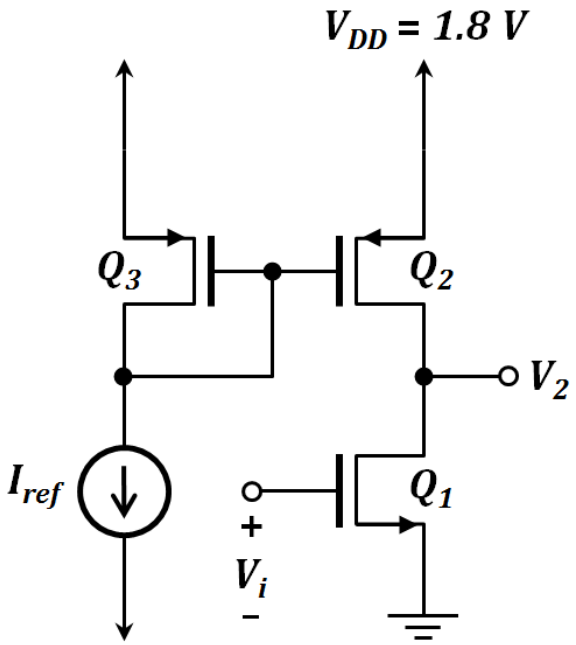

Fig. 1

2 (a) Explain what is meant by an ideal voltage source and an ideal current source. [25%]

(b) Shown in Fig. 2 are two common-base amplifiers, driven by an ideal voltage source Fig. 2 (a) and an ideal current source Fig. 2 (b), respectively.

(i) Assuming that each circuit has been properly biased, and that the biasing networks, which are not indicated in Fig. 2, do not affect the small-signal analysis, calculate the output resistance, r_{out} for circuits (a) and (b), using the following data: $r_\pi = 1\ k\Omega, r_o = 100\ k\Omega$, and $\beta = 100$. [50%]

(ii) Comment on the physical implications of the results for r_{out} for each of the two configurations. [25%]

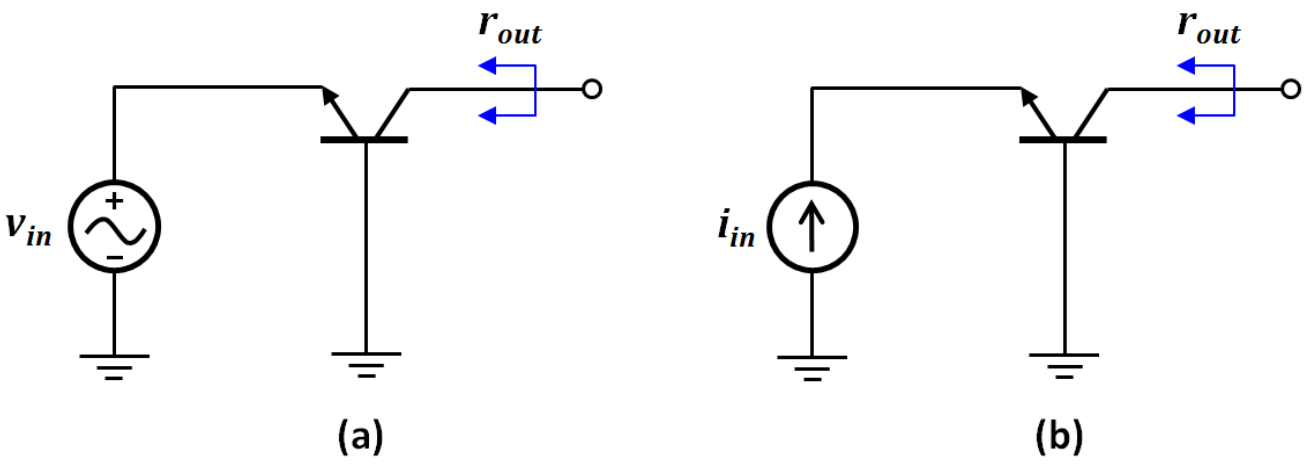

Fig. 2

3 (a) With the aid of circuit block illustrations, define negative feedback, as applied to electronic circuits, describing its effect on circuit characteristics such as gain, linearity, input and output impedances, and bandwidth. [25%]

(b) What are the four negative feedback circuit topologies? State clearly whether the nature of the sampled and mixing signals is a voltage or current as applied to the different amplifier topologies. [25%]

(c) A feedback trans-resistance amplifier circuit is shown in Fig. 3. Assuming $R_F >> R_C$ and $r_o >> R_C$ and that the feedback causes the signal voltage at the input node to be nearly zero:

(i) Derive expressions for $A \equiv V_o/I_i$, $\beta \equiv I_f/V_o$ and $A_f \equiv V_o/I_s$. [30%]

(ii) Find the value of A_f for the case of R_C = 10 kΩ, R_F = 100 kΩ and the transistor current gain β = 100. [20%]

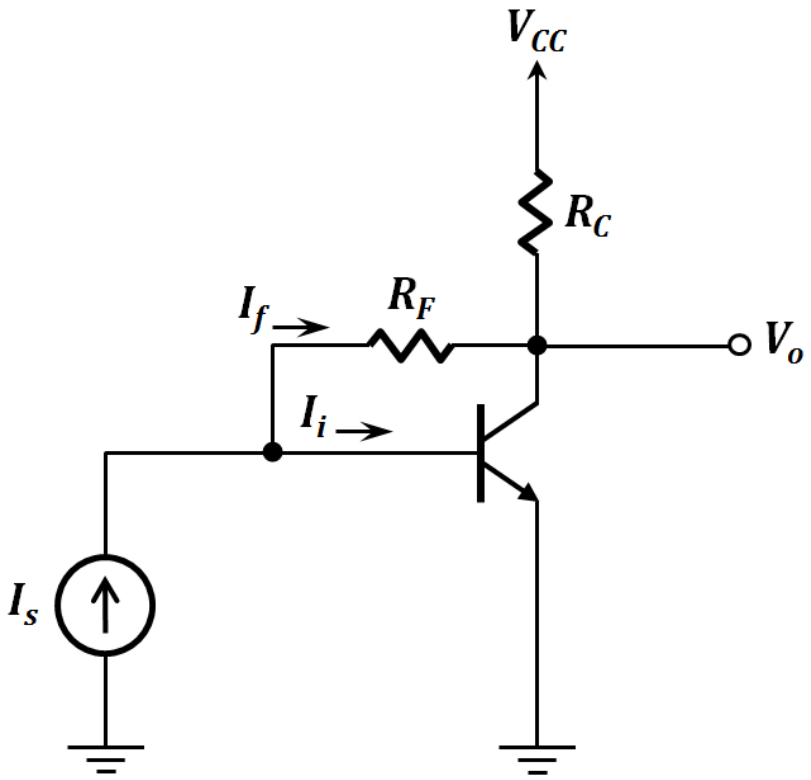

Fig. 3

4 (a) Consider a MOSFET fabricated in 0.18 μm CMOS technology. With the aid of a device schematic, describe the main sources of capacitances (along with typical values) that influence high frequency circuit performance. [25%]

(b) With the aid of a simplified equivalent circuit, show that the MOSFET's unity gain frequency ω_T can be approximated as $\omega_T = g_m /(C_{gs} + C_{gd})$, where g_m is the transconductance, and C_{gs}, C_{gd} the gate-source and gate-drain capacitances, respectively. [15%]

(c) The components in the circuit shown in Fig. 4 have the following parameters: $\mu_n C_{ox}$ (W/L) = 2 mAV^{-2}, V_t = 0.5 V, $C_{gs} = C_{gd}$ = 10 fF, R_1 = 100 kΩ, R_{G1} = 600 kΩ, R_{G2} = 1.4 MΩ, R_D = 2 kΩ, R_L = 10 kΩ, R_S = 1 kΩ and $C_{C1} = C_{C2} = C_S = \infty$. The supply voltage V_{DD} = 1.8V and Early voltage V_A = -26V.

(i) Construct the small signal equivalent circuit. [15%]

(ii) Find the mid band voltage gain v_o/v_i [15%]

(iii) What is the approximate upper -3dB frequency f_H ? [20%]

(iv) Briefly comment, using intuitive-based reasoning, on the circuit's high frequency behaviour in relation to the common-source amplifier. [10%]

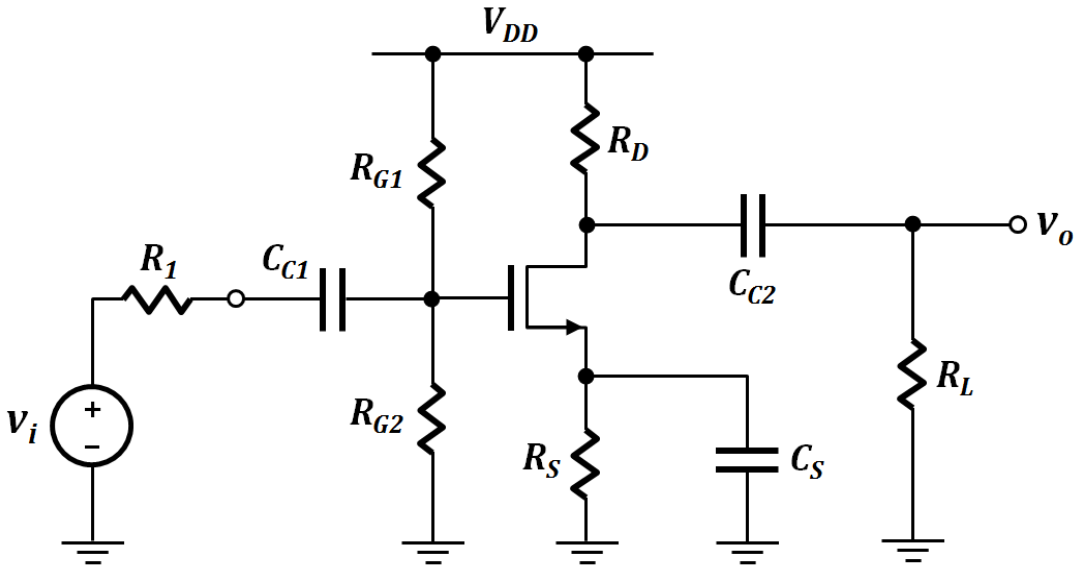

Fig. 4

5 (a) Give a short account of the applications in which integrated *phase-lock loop architectures* are commonly used. [20%]

In a frequency synthesiser design for a computer motherboard, a current-starved Voltage-Controlled Oscillator (VCO) comprising seven identical stages is to be designed, based on the circuit in Fig. 5. The figure shows a single stage of the circuit (comprising transistors *M1*, *M2*, *M3* and *M4*), enclosed in dashed lines, and the current control circuit (*M5* and *M6*).

(b) Complete the schematic circuit for the VCO, and explain its mode of operation, giving details of what determines the frequency of operation. [20%]

(c) The total capacitance being driven at the output node of each stage is 2 fF. Assume that the minimum value of the control voltage V_{inVCO} is equivalent to the threshold voltage for M5. The threshold voltage for all devices has magnitude 1 V. The supply voltage V_{DD} is 5 V, and the maximum drain current in each stage is to be 100 μA. Stating any other assumptions made,

(i) estimate the maximum frequency that can be generated. [10%]

(ii) develop an equation for the VCO gain, K_V, and estimate its value. Comment on the linearity that can be achieved.[20%]

(d) With the help of a block diagram, explain how the VCO developed in parts (b) and (c) could be used in combination with other suitably chosen circuit elements to achieve a frequency synthesiser whose output frequency is to be exactly 4 times the frequency of a stable reference. [30%]

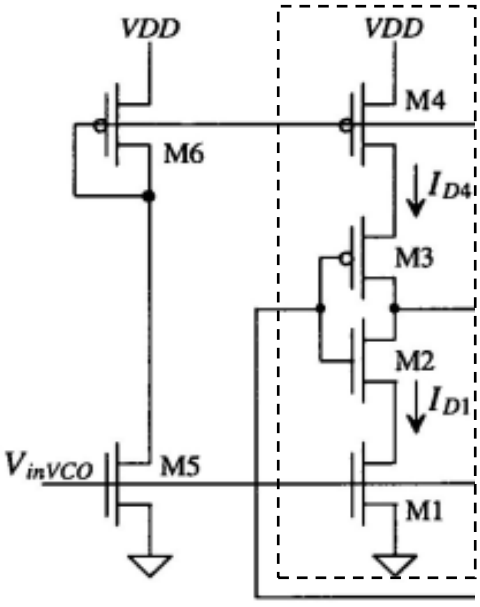

Fig. 5

END OF PAPER

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4B21 ANALOGUE INTEGRATED CIRCUITS DATA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - {v_{DS}}^2] \qquad K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$

$i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad k' = \mu C_{ox}$

$g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm}$

$CMRR = 20\log|A_d / A_{cm}| \qquad A_{cm} = \frac{v_o}{v_{cm}} \qquad A_d = \frac{v_o}{v_d} = g_m R_D$

OR OR

$A_{cm} = \frac{\Delta R_D}{2R} \qquad A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = emitter\ resistance$

FET small signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2} \qquad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1-K) \qquad K \equiv \frac{V_2}{V_1}$

Thermal Noise: $< {v_n}^2 >= 4kTBR \qquad k = 1.38x10^{-23}\ J/K$

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Feedback Architectures and Properties:

	Series-Shunt	**Series-Series**	**Shunt-Series**	**Shunt-Shunt**
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set[1]	$V_o=0$	$I_o=0$	$I_o=0$	$V_o=0$
To find output loop, set[1]	$I_i=0$	$I_i=0$	$V_i=0$	$V_i=0$
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_v = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1+\beta A$	$1+\beta A_v$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
A_f	A_v/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$R_o/(1+\beta A_v)$	$R_o(1+\beta G_M)$	$R_o(1+\beta A_i)$	$R_o/(1+\beta R_M)$
$R'_{of} = R_{of} \lVert R_L$	R'_o/D	$R'_o(1+\beta G_M)/D$	$R'_o(1+\beta A_i)/D$	R'_o/D

[1]This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L, and R_S into account.