Version SS/4

EGT3
ENGINEERING TRIPOS PART IIB

Monday 30 April 2018 9.30 to 11.10

Module 4B21

ANALOGUE INTEGRATED CIRCUITS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Attachment: Formula Sheet (2 pages)
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) What is the advantage of CMOS technology from the point of view of voltage amplifier design with MOSFETs? [30%]

(b) Consider the CMOS active load differential amplifier shown in Fig. 1. The input nodes receive DC voltages V_{IN+} and V_{IN-}. A bias voltage V_B is used for the MOSFET M5 to establish the tail current. For all MOSFETs, the gate oxide capacitance per unit area, C_{ox} = 400 nF/cm^2. The mobility for n-MOSFETs is μ_n = 1000 cm^2/Vs. The mobility for p-MOSFETs is μ_p = 250 cm^2/Vs.

(i) With the inputs V_{IN+} and V_{IN-} grounded, identify the aspect ratios for the MOSFETs M1, M2, M3, M4 and M5 that will result in M1, M2, M3 and M4 each conducting a current of 0.1 mA. Perform the design such that the overdrive voltage (i.e. the absolute value of the difference between the gate-source voltage and the threshold voltage) for each MOSFET is 0.2 V. [35%]

(ii) The small signal output impedance of MOSFETs M1, M2, M3 and M4 due to channel length modulation is 100 kOhm. If the inputs receive small signal input voltages $+v_{in}$ and $-v_{in}$ with the DC level being 0V, what is the small signal, low frequency differential voltage gain? [35%]

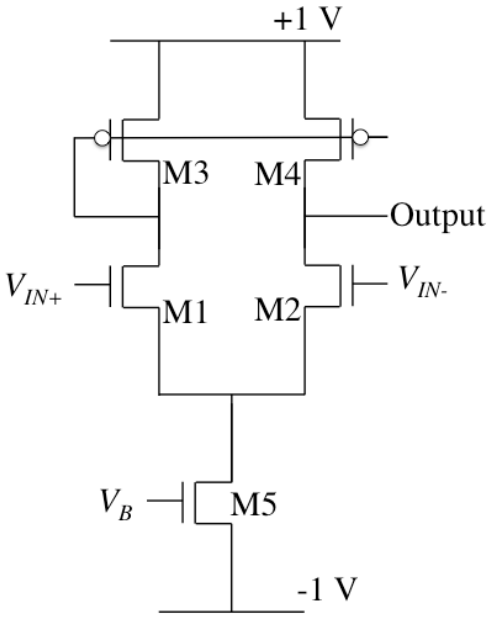

Fig. 1

2 (a) The driver MOSFET of a common source amplifier has a significantly large gate-drain/source overlap capacitance. If the amplifier is designed to have large gain, explain how this might impact the frequency response? [30%]

(b) Consider the multi-stage amplifier circuit shown in Fig. 2. The DC supply voltage is V_{DD}, while v_{in} and v_{out} are the small signal input and output voltage, respectively. All MOSFETs are in saturation mode operation and all BJTs are in active mode operation. Ignore channel length modulation in MOSFETs and base width modulation in BJTs. Transistors Q1, Q2, Q3 and Q4 have transconductance g_{m1}, g_{m2}, g_{m3} and g_{m4} respectively. The parameters n and m are constant coefficients.

(i) What is the small signal, low frequency voltage gain, v_{out}/v_{in}? [35%]

(ii) What is the small signal, low frequency input impedance? [35%]

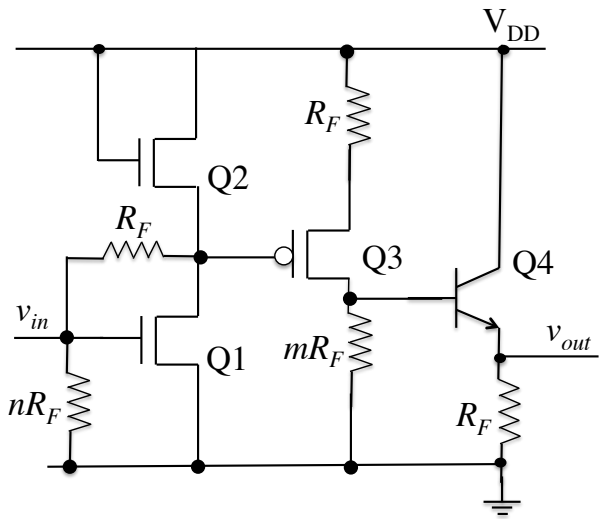

Fig. 2

3 (a) Consider the circuit shown in Fig. 3. MOSFET M1 has an aspect ratio W/L = 2, MOSFETs M2 and M3 have aspect ratio W/L = 1 and MOSFET M4 has an aspect ratio W/L = 4. For all MOSFETs, the threshold voltage is V_t = 1 V, the mobility is μ = 1000 cm^2/Vs and the gate capacitance per unit area is C_{ox} = 40 nF/cm^2. Ignore channel length modulation in all MOSFETs.

(i) If M1 and M2 are to operate as a good current mirror pair, calculate the value of the maximum resistance the resistor R can take. [25%]

(ii) If resistor R has resistance 20 kOhm, what is the DC value of the voltage V_P? [25%]

(iii) If resistor R has resistance 10 kOhm, what is the DC value of the voltage V_{OUT}? [25%]

(b) A two MOSFET current mirror is a useful circuit to generate bias. However, channel length modulation results in inaccuracies. With the aid of a circuit and relevant analysis, explain how a MOSFET cascode current mirror circuits mitigates problems due to channel length modulation. [25%]

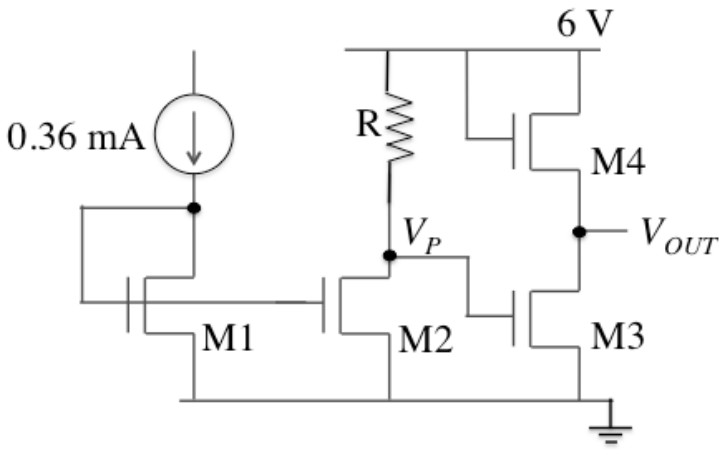

Fig. 3

4 (a) What is meant by the 'corner frequency' of a MOSFET in the context of noise? [20%]

(b) Consider the circuit shown in Fig. 4. The n-channel MOSFET is in above threshold saturation mode of operation and the load resistor has resistance R_L. The DC power supply is V_{DD}. Ignore channel length modulation. How does doubling the aspect ratio of the MOSFET impact the input referred voltage noise? [40%]

(c) In a series resistor-capacitor (RC) circuit, no signal is applied and the only source of noise is the resistor. Analytically prove that the infinite bandwidth noise voltage (in V^2) measured at the junction of the resistor and capacitor is halved when the resistance is halved and capacitance is doubled. [40%]

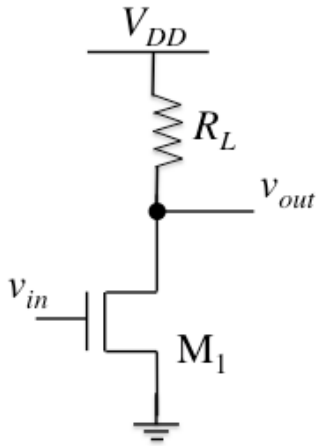

Fig. 4

Answers to Numericals:

1.) b (i) For M1, M2, W/L=12.5
For M3, M4, W/L=50
For M5, W/L=25
(ii) Differential Gain=50

3.) a (i) 16.67kOhm
(ii) 2.5V
(iii) 3.4 V

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FORMULA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - {v_{DS}}^2] \qquad K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$

$i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad k' = \mu C_{ox}$

$g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm}$

$CMRR = 20\log|A_d / A_{cm}| \qquad A_{cm} = \frac{v_o}{v_{cm}} \qquad A_d = \frac{v_o}{v_d} = g_m R_D$

OR OR

$A_{cm} = \frac{\Delta R_D}{2R} \qquad A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$R_{id} = 2(\beta+1)(r_e + R_E)$

R_E = *emitter resistance*

FET small signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$ $i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1 - G)$ $G \equiv Gain$

Noise:

Thermal Noise voltage in resistor (V^2/Hz): $< v_n^2 >= 4kTR$ $k = 1.38x10^{-23} J/K$

Thermal Noise voltage in above threshold MOSFET (V^2/Hz): $< v_n^2 >= 4kT(2/3)(1/g_m)$

Thermal Noise current in above threshold MOSFET (A^2/Hz): $< i_n^2 >= 4kT(2/3)(g_m)$

Flicker Noise in MOSFET (V^2/Hz): $< v_n^2 >= \alpha / (C_{ox}WLf)$

α = Process Dependent Constant Coefficient

Feedback Architectures and Properties:

	Series-Shunt	Series-Series	Shunt-Series	Shunt-Shunt
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set[1]	V_o=0	I_o=0	I_o=0	V_o=0
To find output loop, set[1]	I_i=0	I_i=0	V_i=0	V_i=0
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_v = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_v$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_v / D	G_M / D	A_I / D	R_M / D
R_{if}	$R_i D$	$R_i D$	R_i / D	R_i / D
R_{of}	$R_o / (1 + \beta A_v)$	$R_o(1 + \beta G_M)$	$R_o(1 + \beta A_i)$	$R_o / (1 + \beta R_M)$
$R'_{of} = R_{of} \backslash\backslash R_L$	R'_o / D	$R'_o(1 + \beta G_M) / D$	$R'_o(1 + \beta A_i) / D$	R'_o / D

[1]This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L, and R_S into account.