Version FU/2

EGT3
ENGINEERING TRIPOS PART IIB

Thursday 30 April 2015 9.30 to 11

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Discuss briefly the differences between a Punch-Through (PT) high voltage junction and a Non-Punch-Through (NPT) high voltage junction. Which of the two is preferred in the design of a Bipolar Junction Transistor (BJT) and why? [40%]

(b) Either a power MOSFET or an Insulated Gate Bipolar Transistor (IGBT) are to be used in an inductive application with the current and voltage turn-off waveforms shown schematically in Fig. 1. The rail voltage V_{dc} = 400V and the on-state current required for the application is I_{ON} = 3A. The static and dynamic parameters of the two transistors are summarised in Table 1. Consider that the turn-on and the off-state losses are negligible for both transistors. The switching frequency is variable from 10 kHz to 100 kHz with a constant duty cycle of D = 50%.

Parameter	On-state voltage drop V_{ON} [V]	Turn-off delay time t_s [μs]	Turn-off voltage growth time t_g [μs]	Turn-off current fall time t_f [μs]
Power MOSFET	5	0.1	0.3	0.1
IGBT	2	0.1	0.3	0.6

Table 1

(i) Estimate the total power losses in the Power MOSFET and the IGBT and sketch a graph of these as a function of frequency. Comment on the efficiency of these transistors and the preferred use of one or the other for the given range of frequency (10 kHz to 100 kHz). [40%]

(ii) The parameters in Table 1 are given at room temperature. How would you expect the on-state and the turn-off power losses to change at higher junction temperatures for the two transistors? Will the junction temperature influence the choice of the transistor? [20%]

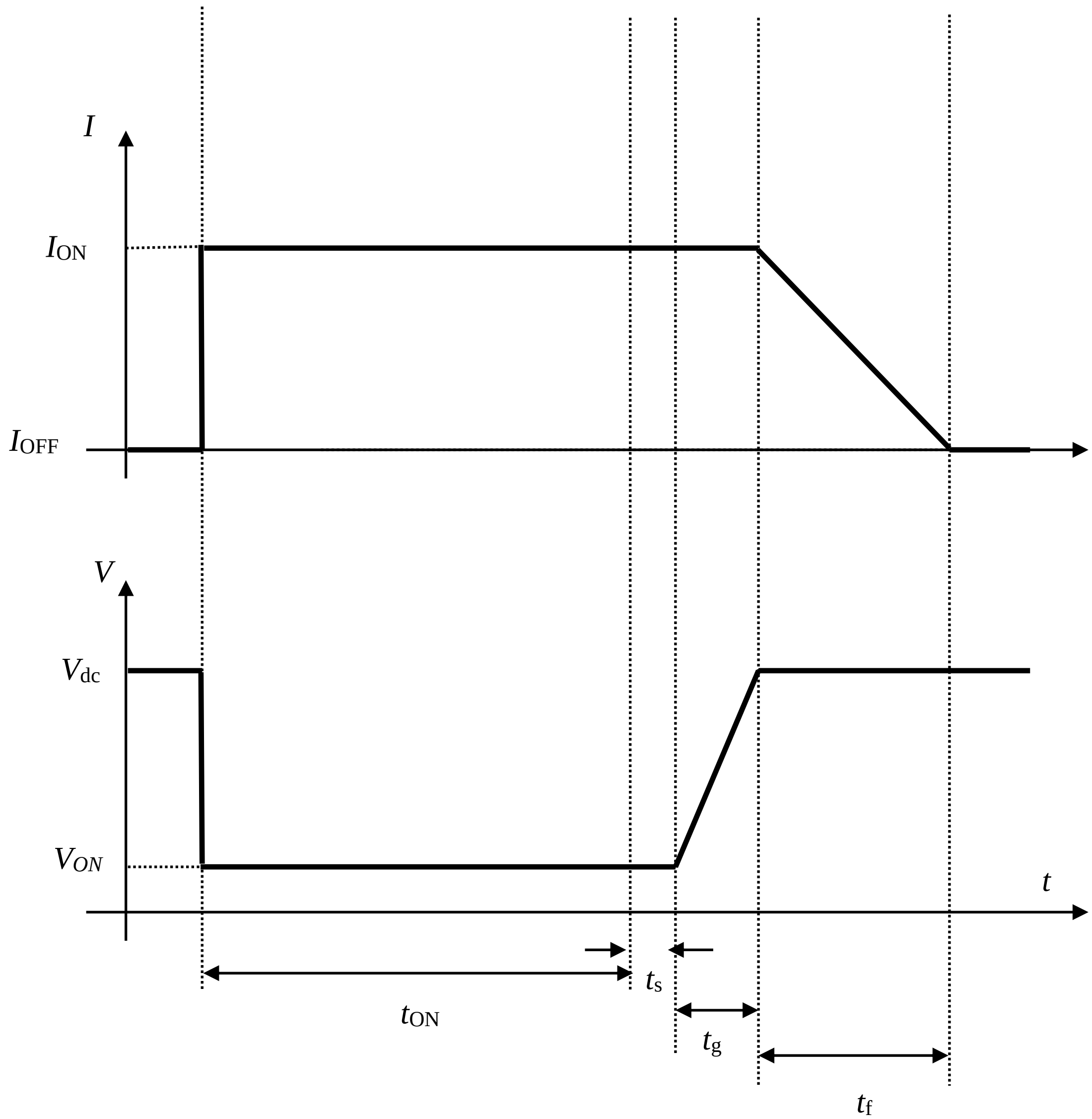

Fig. 1

2 (a) Explain the dI/dt effect in thyristors. Give two solutions to improve the dI/dt ratings and discuss their advantages and disadvantages. [30%]

(b) (i) Using the simplified Ebers-Moll equivalent models for the two bipolar transistor components of the thyristor, find an expression for the anode current in the voltage blocking mode as a function of the leakage currents of the bipolar transistors and their current gains α_{npn} and α_{pnp}. [30%]

(ii) Calculate the break-over voltage, V_{BO}, of a thyristor, assuming that the current gain, α_{npn}= 0.5 and remains constant. The width of the n-drift region w_{drift} = 200 μm, the hole diffusion length Lp = 50 μm and the doping concentration of the n-drift region, $N_D = 10^{13}\ cm^{-3}$. [30%]

(iii) Discuss briefly the occurrence of break-over and avalanche breakdowns in the drift region of a thyristor and that of a PIN diode. [10%]

You may assume the following equations in the calculations of breakdown and current gain of a pnp transistor

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

$$\alpha_{pnp} \approx 1 - \frac{w_{eff}^{\ 2}}{2L_p^{\ 2}}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, α_{pnp} is the current gain of the pnp transistor, w_{eff} is the effective base width of the pnp transistor, L_p is the hole diffusion length, q is the electronic charge and the other symbols have their usual meaning. $\varepsilon_0 = 8.854 \times 10^{-12}\, F/m$, ε_r =11.9 for Silicon.

3 The structure in Fig. 2 is a MOS controllable power device with a trench gate.

(a) Explain briefly its operation during on-state, off-state, turn-on and turn-off. Discuss specifically the roles of the *n well* and the *deep p+* region and comment on the design of these regions for an efficient operation of the device. [50%]

(b) Give two advantages and two disadvantages of this device compared to a conventional Trench Insulated Gate Bipolar Transistor (TIGBT). [20%]

(c) Draw a termination structure based on trenches and deep p+ regions and explain its effect in eliminating the premature breakdown at the edge of the device. [30%]

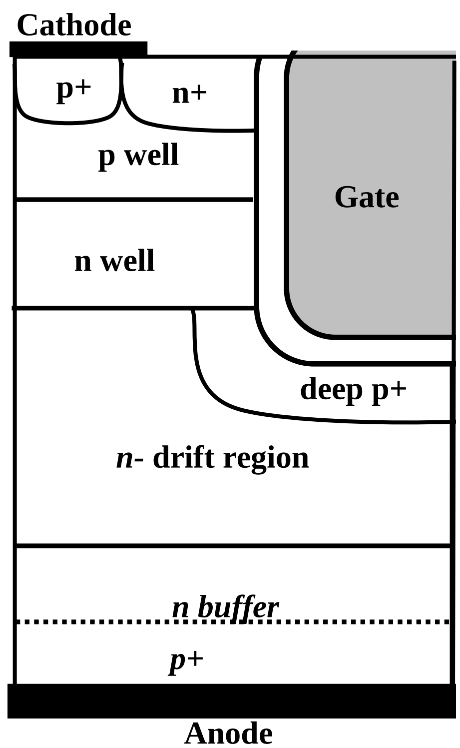

Fig. 2

4 (a) (i) Draw the structure of the Cool MOS and explain its advantage in terms of the trade-off between the specific on-state resistance and the breakdown voltage. [25%]

(ii) Draw schematically a graph of the drain-source capacitances as a function of the blocking voltage for both the Cool MOS and a conventional power MOSFET. Explain briefly the different characteristics with respect to voltage of the two capacitances at low voltages and high voltages. [25%]

(b) Some of the main physical properties for Silicon and wide bandgap materials are given in Table 2.

(i) Explain why Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond are attractive materials for power devices. Give two advantages and two disadvantages for each of these materials when compared to silicon. [25%]

(ii) Calculate the percentage reduction in the on-state resistance for a classical power MOSFET in SiC when compared to a classical power MOSFET in Si for a 1.2 kV rated device. Comment on the result if the rating of the device is 100 V instead of 1.2 kV. [25%]

You may assume the following equation in the calculation of the breakdown voltage

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, q is the electronic charge and the other symbols have their usual meaning.

Property	**Si**	**SiC**	**GaN**	**Diamond**
Band gap (eV)	1.1	3.2	3.4	5.5
Relative permittivity	11.9	10	9.5	5.7
Breakdown field (MV/cm)	0.3	3	3.3	5
Thermal conductivity (W/K/cm)	1.48	3.30	1.30	24.00
Mobility ($cm^2/(Vs)$)	1350 for electrons	700 for electrons	2000 for electrons	3800 for holes 4500 for electrons
Saturation velocity (10^7cm/s)	1	2	2.5	2

Table 2

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Engineering Tripos Part II B
Numerical Anwers, Module 4B2 - 2015

Q1.

(b)
Total losses in MOSFET $7.5 + 246 \times 10^{-6} f$ (W)
Total losses in IGBT $3 + 543.3 \times 10^{-6} f$ (W)

Intersection point: 15.1 kHz

Q2.

(b) (ii) breakover voltage V= 170.83 V

Q4.

(b) (ii) $R_{onSi} = 435.73\ R_{onSiC}$