Version FU/5

EGT3
ENGINEERING TRIPOS PART IIB

Wednesday 20 April 2016 2 to 3.30

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) With the help of a schematic cross-section of a device, describe the stored charge levels during active region, quasi-saturation region, hard saturation region and deep saturation region in a high voltage Bipolar Junction Transistor (BJT) Show these regions on a graph of the forward-biased characteristics of the BJT. [30%]

(b) A Non Punch Through (NPT) Insulated Gate Bipolar Transistor (IGBT) is to be used in an inductive application with the current and voltage turn-off waveforms shown schematically in Fig. 1. The rail voltage is V_{dc} = 400V and the on-state current required for the application is I_{ON} = 10A. The static and dynamic parameters at 25 ^{o}C of the NPT IGBT are summarised in Table 1. Consider that the turn-on and the off-state losses are negligible. The duty cycle is D = 50% and the current level at the start of the turn-off tail is I_{tail} = 2A.

Parameter	On-state voltage drop V_{ON} [V]	Turn-off delay time t_s [μs]	Turn-off voltage growth time t_g [μs]	Fast turn-off current fall time t_{f1} [μs]	Tail turn-off current fall time t_{f2} [μs]
Value	2	0.1	0.3	0.2	1

Table1

(i) Explain the physical reason for the long turn-off tail of the NPT IGBT. [10%]

(ii) Estimate the maximum allowable operating frequency to ensure that the device turns off completely during the turn-off process. [10%]

(iii) Estimate the maximum allowable operating frequency for the maximum temperature not to exceed the junction temperature T_j = 175 ^{o}C. Consider the ambient temperature to be 25 ^{o}C, and the thermal resistance from ambient to junction to be R_{thja}= 7.5 °C/W. Assume that the parameter values given in Table 1 do not change with temperature. [40%]

(cont.

(iv) How would you expect the result in part (iii) to change if the parameter values in Table 1 change with the increase in the junction temperature? Justify your answer and state any assumptions made. [10%]

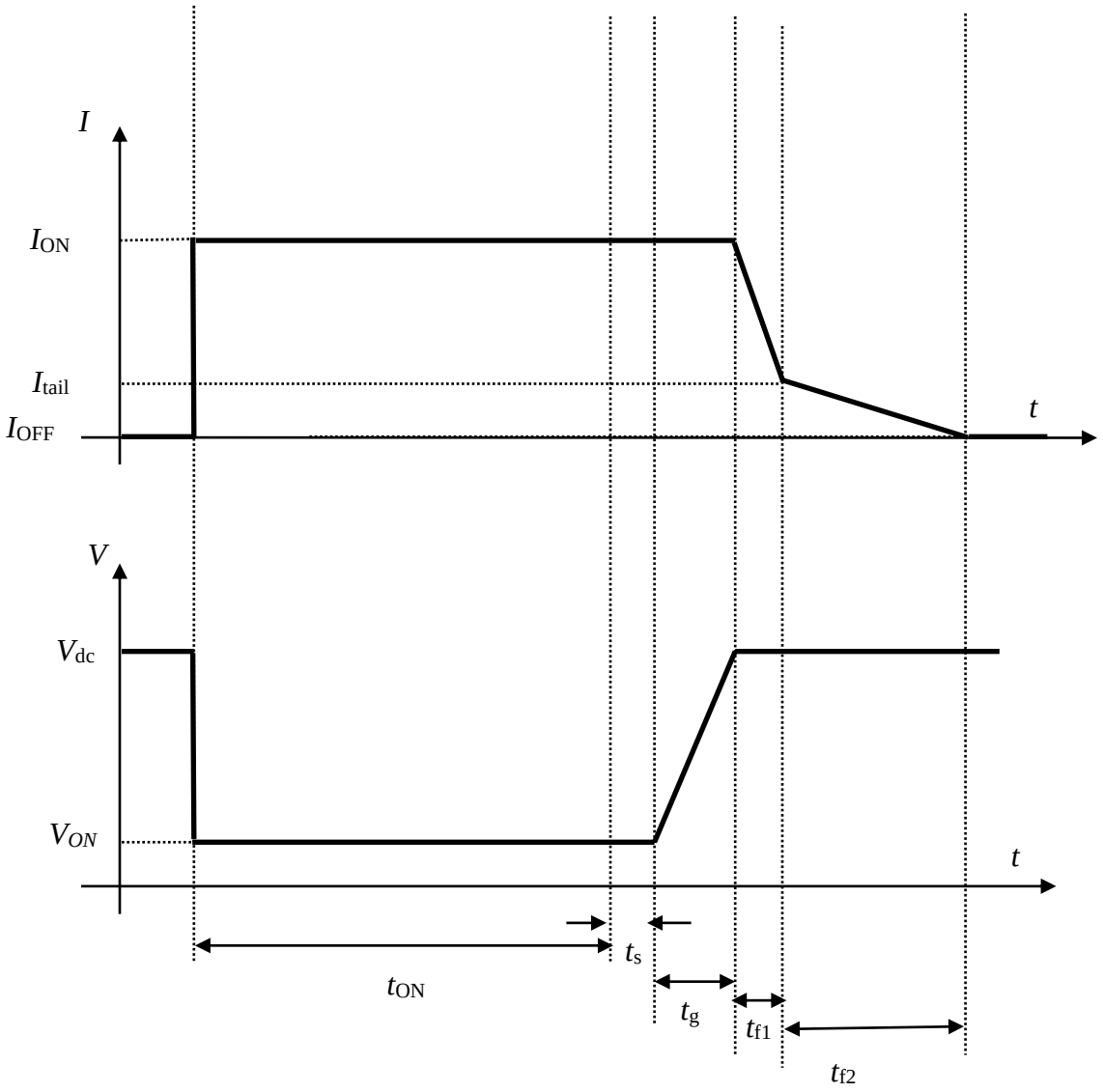

Fig. 1

2 (a) Draw schematically a cross-section of a Reduced Surface Field Lateral Insulated Gate Bipolar Transistor (RESURF LIGBT) and explain its operation. Briefly describe its advantages and disadvantages compared to a RESURF Lateral Diffused MOSFET (LDMOSFET). [30%]

(b) Explain the dV/dt effect in thyristors. Give two solutions to improve the dV/dt rating and discuss their advantages and disadvantages. [30%]

(c) Using the simplified equivalent model of a Gate Turn Off (GTO) thyristor, find an expression for the minimum gate current needed to turn off successfully the thyristor as a function of the on-state anode current I_A and the current gains of the npn and pnp bipolar transistors, α_{npn} and α_{pnp} respectively. [30%]

What design choices in the GTO may be made to minimise the turn-off gate current? [10%]

[Hint: Consider that to turn off successfully the thyristor, the current at the base terminal of the npn transistor should become smaller than its on-state collector current divided by the on-state amplification gain β_{npn}.]

You may assume the following definitions for the current gain α and the transistor amplification gain β:

$$\alpha = \frac{I_C}{I_E} \qquad \beta = \frac{I_C}{I_B}$$

where and I_C, I_E, I_B are the Collector, Emitter and Base current of a bipolar transistor respectively.

3 The structure in Fig. 2 is a MOS controllable power device with a trench gate.

(a) Explain briefly its operation during on-state, off-state, turn-on and turn-off. Discuss specifically the roles of the 'n well', the 'n drift' and 'p drift' regions and comment on the design of these layers including their doping charge levels and geometrical dimensions for an efficient operation of the device. [60%]

(b) Give two advantages and two disadvantages of this device compared to a conventional Trench Insulated Gate Bipolar Transistor (TIGBT). [20%]

(c) Give two advantages and two disadvantages of this device compared to a Cool MOS transistor. [20%]

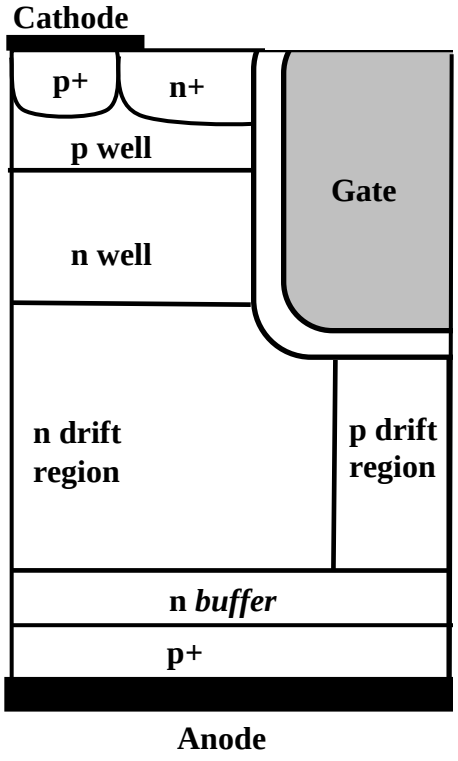

Fig. 2

4 (a) Draw schematically an AC to DC converter in a Switch Mode Power Supply (SMPS). Describe its operation and discuss its advantages and disadvantages compared to an AC to DC converter using linear electronics. [30%]

(b) Using a simplified equivalent circuit find the output voltage as a function of the rectified input voltage, the duty cycle and the turn ratio of the transformer for an AC to DC converter in a SMPS. State any assumptions made. [20%]

(c) A PIN fast recovery diode is rated at 100A, 1200V and 150 °C. It is to be turned off from a forward current of 72A with a *di/dt* of 25A/μs. The data sheet states that the recovered charge is 0.6μC at a temperature of 25 °C. All the charge is assumed to be stored charge.

(i) Calculate the maximum reverse recovery current and the effective time taken for the reverse recovery t_{rr}. [40%]

(ii) Explain how these will change if the temperature is increased to the maximum temperature of 150 °C. [10%]

.

END OF PAPER

ENGINEERING TRIPOS PART IIB 2016
4B2 Numerical Solutions

Q1: (b) (ii) f_{max} = 312.5 kHz
(b) (iii) f =6.73 kHz

Q2 (c) the turn-off condition: $I_G > \frac{I_A}{G}$ where G is called the turn-off gain with $G = \frac{\alpha_{npn}}{\alpha_{npn} + \alpha_{pnp} - 1}$

Q4 (b) $V_0 = \frac{N_2}{N_1} V_d \frac{t_{ON}}{T_S}$

(c) (i)

t_{rr} = 0.21 μs
Irm = 5.46A