Version DMH/4

EGT3
ENGINEERING TRIPOS PART IIB

Friday 24 April 2015 2 to 3.30

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) How would you define *yield* in Integrated Circuit (IC) manufacturing? [15%]

(b) Briefly describe five factors that affect yield. [30%]

(c) Consider a die whose area is 6 mm x 6 mm with a defect density of 0.7 cm^{-2}. The die includes an analogue section of 100 transistors whose characteristics must be matched to within 0.5% of the die average value. Assume that the matching characteristics of the transistors are dominated by a single parameter, which follows a normal distribution with a $\pm 3\sigma$ window characterised by a variation from the die average of +0.5%.

(i) Determine the yield using Seed's model if the soft faults in the analogue section are neglected. [20%]

(ii) Estimate the yield if both hard and soft faults are considered. [20%]

(d) Comment on the physical implications of your results in part (c). [15%]

2 (a) Describe the types of information that can be obtained by scanning a focused electron beam across a silicon CMOS circuit. Why is secondary electron imaging more sensitive to surface features than backscattered electron imaging? How can circuits operating normally be examined with an electron beam? [40%]

(b) A constant-field scaling operation is applied to the design of a CMOS logic circuit such that lateral dimensions in the devices and interconnections are shrunk by a factor k which is greater than, but close to, unity. Describe the predicted effect of this procedure on the following circuit parameters:

(i) parasitic capacitances and resistances [20%]

(ii) speed of operation [10%]

(iii) current and power consumption. [10%]

(c) Summarise the potentially beneficial and adverse effects of scaling a design in the way described in part (b). [20%]

3 (a) What is the definition of the *threshold voltage* in a MOSFET? Discuss briefly the major physical and other factors that determine the threshold voltage in a MOSFET. [30%]

(b) The *flash memory* relies for its operation on varying the threshold voltage of a form of MOSFET by electrical means.

(i) With the aid of a diagram to show the structure of a flash memory cell, explain how this is accomplished. [20%]

(ii) Hence outline the mode of operation of the flash memory cell, and describe the steps involved in writing data to the device and reading it back. [35%]

(iii) What are the main advantages and disadvantages of this approach compared with other MOS implementations of high density memory? [15%]

4 (a) Describe the primary causes of dissipation of electrical power in a CMOS digital integrated circuit. Discuss the circumstances and classes of circuits in which they are important. [20%]

(b) What are the means available to the IC designer to reduce the energy consumption of a full-custom CMOS digital integrated circuit? In your account you should refer to process and device selection, as well as to any circuit techniques and abstractions by which economy of power may be optimised. [20%]

(c) In a multimedia application, the input data-path of a streaming digital multimedia processor is implemented as an integrated module using a 0.5 μm CMOS process. This module may be modelled as a large array of 40,000 memory elements, organised as a set of twenty 2,000-bit shift registers. Binary data sequences are accepted at twenty input pins, and are applied to the serial inputs of the shift registers. The shift registers operate continuously, clocking data serially from input to output and are driven with a 100 MHz clock to all stages. On appearing at the serial outputs, the data patterns are presented to the processor itself.

Each memory element of the array drives a load which may be assumed to be purely capacitive and equivalent to 10 fF. By considering the dynamic power dissipated in the shift-register array as data are clocked through, estimate the worst-case current consumption of that part of the circuit, assuming that the supply V_{DD} is 3.0 V. For this calculation you may ignore power losses due to other mechanisms. State any other assumptions made. [30%]

(d) Discuss briefly the potential inaccuracies introduced in (c) by neglecting losses due to other mechanisms. [15%]

(e) The processor described in part (c) is to be adapted for an application in which power consumption must be minimised. Briefly outline the options available to the designer to achieve this. [15%]

5. (a) Describe the circuit and mode of operation of a transmission gate in CMOS technology, and explain clearly how this circuit may provide performance superior to that of a simple pass transistor. [25%]

Give examples of the use of transmission gates in digital circuits, briefly indicating any advantages and disadvantages of the circuit in these applications. [15%]

(b) Explain the origin of *body effect*, or *back-gating*, as encountered with MOS transistors. How does this phenomenon affect the measured characteristics of a transistor? [20%]

By considering circuits for:

(i) a 2-input CMOS NAND gate

(ii) a 2-input CMOS NOR gate,

explain qualitatively how body effect influences the static transfer function and the gate delay observed in these gates. [20%]

What measures are available to the integrated circuit designer to alleviate these difficulties? [20%]

END OF PAPER

Answers

Q1. Hard yield = 60.5 %; overall yield = 46 %.
Hard and soft faults: overall yield = 3.5×10^{-5} %

Q4. Worst-case current = 0.06 A