Version DMH/3

EGT3
ENGINEERING TRIPOS PART IIB

Thursday 28 April 2016 9.30 to 11

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1. (a) What is *yield* and why is it so important in Integrated Circuit (IC) manufacturing? [20%]

(b) Briefly describe *soft* and *hard faults* in analogue and digital ICs. [20%]

(c) What is meant by the *capability index* C_P? State the probability that a fabricated device parameter lies inside the specified design process window. [20%]

(d) If 1000 devices on a chip must have a specific parameter within the specified design process window, determine the soft yield if the process has been characterised by a capability index of:

(i) $C_P = 0.5$

(ii) $C_P = 1.0$

(iii) $C_P = 1.5$

(iv) $C_P = 2.0$ [30%]

(e) Comment on the physical implications of your result in part (d) above. [10%]

You may use the following equations which define models used to predict yield.

The probability P_{die} that a given die is good is given by:

(Seed Model) $$P_{die} = e^{-\sqrt{AD}}$$

(Murphy Model) $$P_{die} = \left(\frac{1 - e^{-AD}}{AD} \right)^2$$

where A = die area and D = average defect density.

The probability P that a parameter lies within the specification design process window is given by:

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3Cp}^{3Cp} \mathrm{e}^{-x^2/2} \, dx$$

where $$f(x) = \frac{1}{\sqrt{2\pi}} e^{-x^2/2}$$ is the probability distribution function for the standard normal distribution.

2. (a) What is the meaning of the term *clock skew* in the context of digital VLSI designs using CMOS technology? [10%]

(b) Draw a diagram to show how a form of 1-bit dynamic memory cell may be constructed using only a single MOS transistor and parasitic capacitance elements. Describe briefly how your circuit operates for *read* and *write* operations. [30%]

(c) Explain how the phenomenon of charge sharing may lead to incorrect operation of a dynamic memory cell. Deduce an appropriate condition, based on estimation of capacitances, which will ensure satisfactory operation. What measures are taken in the design and fabrication of practical dynamic memories to minimise these kinds of problem? [30%]

(d) The storage element in a dynamic memory has capacitance 60 fF and is charged to 5 V. A leakage current of 0.1 nA flows from the storage element to the substrate. Stating any assumptions made, estimate how frequently the data stored in the memory needs to be refreshed. The storage element is switched onto a bit sense line of capacitance 1.5 pF, precharged to 2.5 V. What is the instantaneous change in potential observed on the sense line? [30%]

3 A plan view showing an n-channel MOS transistor and associated interconnect structures is shown in Fig. 1. The polysilicon interconnect and gate electrode *G* are of width 1 μm, and the metal interconnect at *D* and at V_{SS} is of width 2 μm. The interconnect lengths are as shown in the figure. The active region of the transistor, shown dashed, has dimensions 2 μm × 10 μm.

(a) Discuss briefly the origins of the key contributions to parasitic capacitances arising from the MOS device itself and the associated interconnect. [30%]

(b) Table 1 is a table of information abstracted from the manufacturer's data about the process in use, and consists of specific capacitance values per unit area or per unit length. Using the data supplied, determine as accurately as possible the key capacitances at zero bias for this device at input and output. You may ignore the effects of contact structures for the purpose of this calculation. [40%]

(c) Indicate qualitatively how these capacitances would be expected to change if normal device operating voltages were applied. State any assumptions made. [10%]

(d) Draw a cross section through the transistor structure along the dashed line A-A', and identify the various conducting layers and their electrical function in the device. [20%]

Parameter	Value	Units	Description
$\mathbf{C_O}$	5×10^{-4}	Fm^{-2}	Capacitance associated with gate oxide dielectric
$\mathbf{C_{JA0}}$	1×10^{-4}	Fm^{-2}	Area capacitance to substrate (source or drain)
$\mathbf{C_{JP0}}$	4×10^{-10}	Fm^{-1}	Peripheral capacitance to substrate (source or drain)
$\mathbf{C_{GD0}}$	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with drain
$\mathbf{C_{GS0}}$	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with source
$\mathbf{C_{MA}}$	3×10^{-5}	Fm^{-2}	Area capacitance to substrate of metal over field oxide
$\mathbf{C_{MP}}$	4×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of metal over field oxide
$\mathbf{C_{PA}}$	4×10^{-5}	Fm^{-2}	Area capacitance to substrate of polysilicon over field oxide
$\mathbf{C_{PP}}$	5×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of polysilicon over field oxide

Table 1

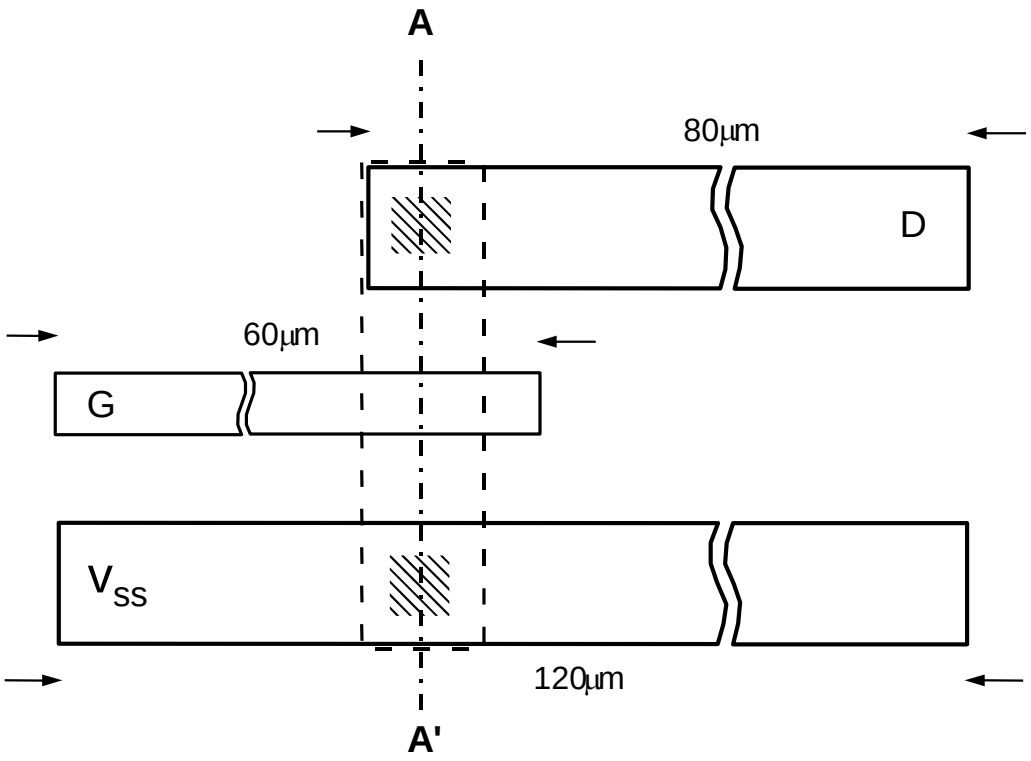

Fig. 1

4 (a) Show that the conductance G of a MOS transistor of aspect ratio W/L in the ON state can be approximated by the expression:

$$G = \mu C_{OX} V_{DD} (W / L)$$

where μ is the electron mobility, C_{OX} is the capacitance per unit area of the gate and V_{DD} is the power supply voltage. [20%]

(b) A multi-stage CMOS output pad driver consists of a number of appropriately designed inverters connected in cascade. It is to transmit the signal from the output of an inverting gate consisting of minimum geometry transistors to a pad, which, together with external circuitry, imposes a purely capacitive load of 75 pF. The capacitance to substrate at the input to the inverting gate is 0.2 pF, and the channel dimensions W and L of the n-channel transistor used in its construction are 1 μm and 0.5 μm respectively.

(i) Estimate the delay that would be observed if the output of the minimum geometry inverter were connected directly to the output pad. [20%]

(ii) Explain how the use of a multi-stage pad driver can be advantageous in achieving the minimum possible delay without occupying excessive area. [20%]

(iii) Stating any assumptions made, show how to find the number of stages required in the driver to minimise the delay, and estimate the minimum delay achieved. [40%]

You may assume that circuit capacitances are dominated by the pad and transistor gate electrode capacitances, and that the delay imposed on a signal by a CMOS inverter driving a capacitive load C is given by $3C/G$, where G represents the conductance of the MOS devices involved. Take $\mu_N / \mu_P = 2$, $\mu_N C_{OX} = 10^{-4}$ AV^{-2} and $V_{DD} = 3$ V.

5. (a) Explain the meaning of the term *scaling* as applied to the design of CMOS integrated circuits. Discuss, with reasons, any parameters other than device dimensions that may need to be adjusted as part of the scaling process. [20%]

(b) In a design conference a few years ago, a designer was asked to consider which of two available CMOS fabrication processes to use for a new design intended to operate at the highest possible frequency. The design was primarily digital, but also contained in addition a number of linear circuit elements. The processes were:

(i) an established process with minimum gate width 0.18 μm and 2.5 V rated power supply;

(ii) a new, scaled process with minimum gate width 0.13 μm and 1.1 V rated power supply.

Write a brief report as might have been presented at the conference, detailing the advantages and disadvantages of the two processes.

Your report should take account of the different structures typically present in such a design and should make reference to packing density, cost, yield, capacitance, current, power consumption and delay as well as any other factors you consider important. [80%]

END OF PAPER

Answers

1. (d)

(i) $C_P = 0.5 \rightarrow P \sim 0.8664$. The probability that all 1000 devices have a parameter within the design spec window is $P^{1000} = (0.8664)^{1000} \rightarrow 0$, and hence the yield => 0%.

(ii) $C_P = 1.0 \rightarrow P \sim 0.9973$, yield = 6.7%.

(iii) $C_P = 1.5 \rightarrow P \sim 0.999993$, yield = 99.3%.

(iv) $C_P = 2.0 \rightarrow P \sim 0.999999998$, yield => 100%.

2. (c)

Minimum refresh time = 1.5 ms

Change in potential observed = 96 mV.

3. (b)

C_{input} = 10.1 fF

C_{output} = 18.7 fF.

4. (b)

(i) τ_{direct} = 375 nS

(ii) Number of stages = 6

Total delay = 13.5 ns.

5.