Version DMH/3

EGT3
ENGINEERING TRIPOS PART IIB

Friday 5 May 2017 9.30 to 11

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) List the main features of Complementary Metal-Oxide-Semiconductor (CMOS) circuit technology and explain why it has displaced other contending technologies for integrated circuits. [30%]

(b) The CMOS circuit whose layout is shown in Fig. 1 is fabricated on an n-type wafer using p-well technology. The line labelled *D* represents the power supply V_{dd}, and the line *F* is the ground V_{ss}.

(i) Indicate (giving coordinates) which of the four implanted regions are implanted with p-type impurities and which are implanted with n-type impurities. [10%]

(ii) Draw a cross section through the device along the line y=26 from x=0 to x=90. Label all relevant conductor and insulator layers in the diagram and list their functions. [20%]

(iii) Describe briefly what is meant by self-aligned transistor technology, and explain which lithography steps are most important in determining the device switching speed. [10%]

(c) (i) Explain briefly what governs the electrical width of the transistors in Fig. 1. [10%]

(ii) By means of measurements taken from Fig. 1, find the designed ratio of the p-channel transistor width to the n-channel width. [10%]

(iii) In the technology to be used, the n-channel mobility is exactly twice the p-channel transistor mobility. Using your measurements from Fig. 1, determine the expected ratio of the worst-case rise time to the worst-case fall time of the output for the circuit. [10%]

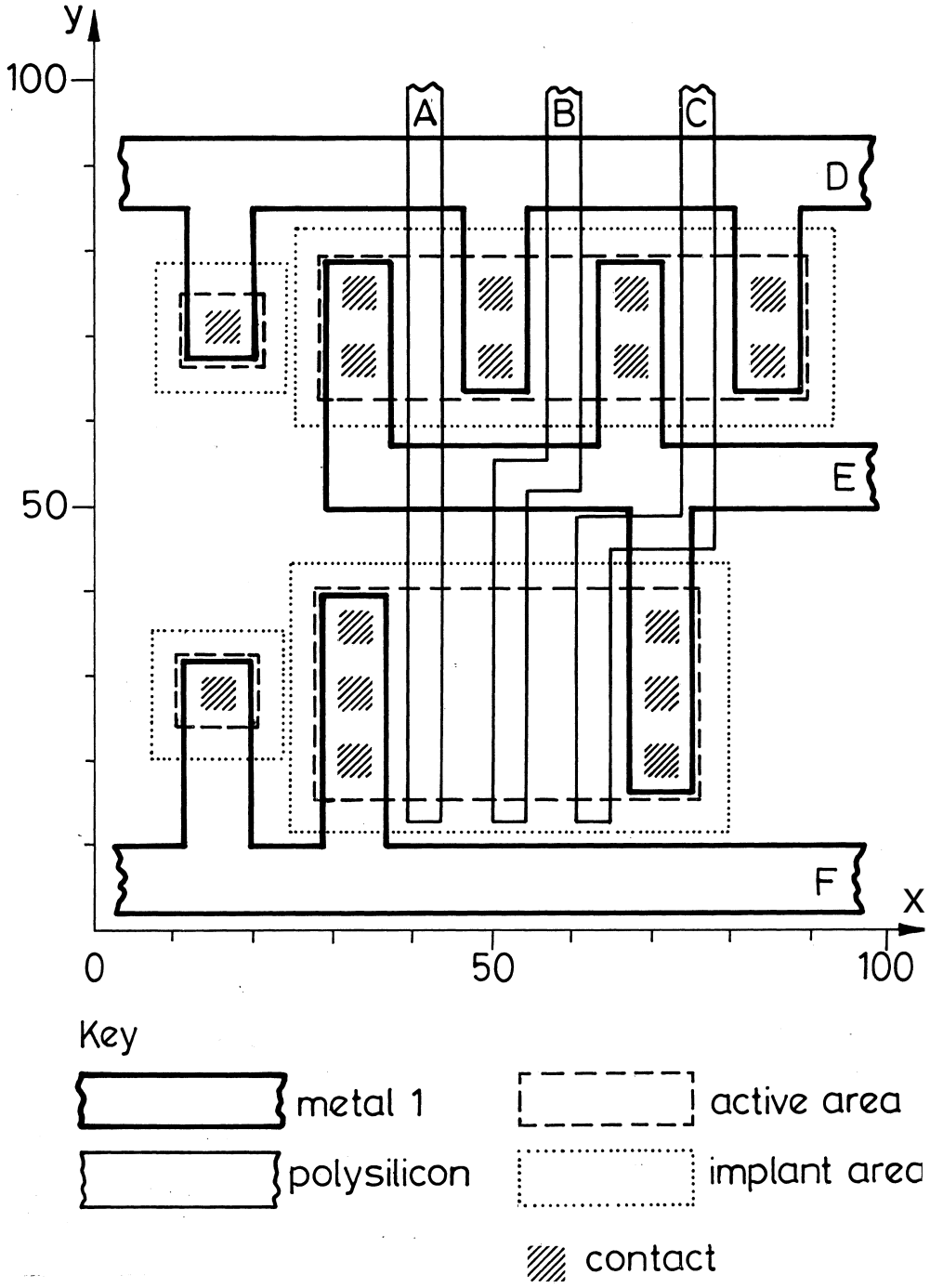
y
100
50
0
50
100
x
A
B
C
D
E
F
Key
metal 1
polysilicon
active area
implant area
contact

Figure 1

2. (a) Scaling of transistors to smaller dimensions generally brings undesired effects associated with device performance. Describe five adverse effects of scaling. [20%]

(b) (i) In VLSI technology, there is a strong desire to run circuits at higher clock speeds. Besides the obvious route of scaling feature sizes to attain higher operating speeds, the silicon on insulator or SOI technology can provide significant speed improvements at reduced power consumption. Describe, with the aid of illustrations, three SOI process technologies that are commonly used in the IC industry. [40%]

(ii) Discuss the uses of SiO_2-based gate dielectrics, referring to the issues related to scaling of the gate dielectric dimensions, and the requirements that new dielectrics must meet for compatibility with Si technology. [40%]

3. (a) Explain the meaning of the term *sheet resistance*. Show how this concept can be used during the design of an integrated circuit to predict the resistance of electrical interconnects containing linear elements and a number of right-angle bends. [30%]

(b) Give a brief explanation of the phenomenon of *electromigration* and the factors affecting its occurrence. What steps can the integrated circuit designer take to alleviate its effects? [30%]

(c) Describe the circuit structures used in CMOS technology to convey digital signals between input pads and the inputs of logic gates comprising small geometry devices. Discuss the precautions used to protect inputs from the effects of applying excessive voltages and static discharges, and to guard against latchup. [40%]

4 (a) What is meant by the term *design rule* in CMOS integrated circuit design? Write a short account of the ways in which design rules constrain the form and dimensions of interconnect and contact structures in CMOS technologies. In your account, indicate the origins of the rules you introduce, making it clear whether they arise from physical, electrical or processing constraints. **Note**: details of specific manufacturers' rules are not required. [50%]

(b) An echo cancellation unit for use in a multimedia application implemented as a CMOS integrated circuit uses a large array of 120,000 memory elements organised as a set of eight 15,000-bit shift registers. All stages of the shift register are driven with a 60 MHz clock. Each memory element drives a load which is purely capacitive and equivalent to 20 fF. Binary data sequences are accepted in parallel at eight input pins, and after passing through the shift register, are presented at eight outputs.

(i) By considering the dynamic power dissipated in the array as data sequences are clocked through, estimate the worst-case current consumption of the array, assuming that the supply V_{DD} is 3.3 V. You may ignore power consumed by input/output pads and other parts of the chip. State any other assumptions made. [30%]

(ii) Electrical power for the shift register array is supplied by means of aluminium interconnect of layer thickness 0.4 μm. Assuming that significant electromigration may be expected to occur in aluminium interconnect at current densities in excess of 10^9 Am^{-2}, determine a suitable width for the interconnect used to supply the required current, stating any assumptions made. [20%]

5. (a) What is the meaning of the term *clock skew* in the context of VLSI designs using CMOS technology, and from what sources does it originate? Briefly discuss the measures that must be taken by IC designers to minimise the effects of clock skew in digital designs. [30%]

(b) In a microcontroller circuit, a clock buffer distributes a single-phase clock signal to a remote part of the circuit by means of a bus consisting of uniform polysilicon interconnect. The length and width of the interconnect are 10 mm and 1 μm respectively; the sheet resistance of the polysilicon is 60 Ω/square, and the capacitance per unit length is 2×10^{-10} F m^{-1}.

Estimate the delay incurred by the signal in propagating the length of the bus. [15%]

Describe carefully how the delay would be affected if:

(i) the width of the interconnect were doubled; [15%]

(ii) a 'salicide' manufacturing process were used, reducing the sheet resistance of polysilicon to 10 Ω/square. [10%]

(c) Inverting buffers are available with delay properties shown graphically and algebraically in Fig. 2. Suggest a suitable amendment to the original polysilicon bus arrangement in (b) that will reduce the delay by at least a factor 2, noting that a non-inverted clock is required at the remote end of the bus. [30%]

Assume that the delay in each buffer depends only on the load capacitance it drives, and that all capacitances other than those due to interconnections can be ignored.

The following expression may be assumed for the propagation delay T of a pulse transmitted along a resistive conductor of length l:

$$T = 0.5\, rcl^2$$

where r represents the resistance per unit length, and c represents the capacitance to substrate per unit length.

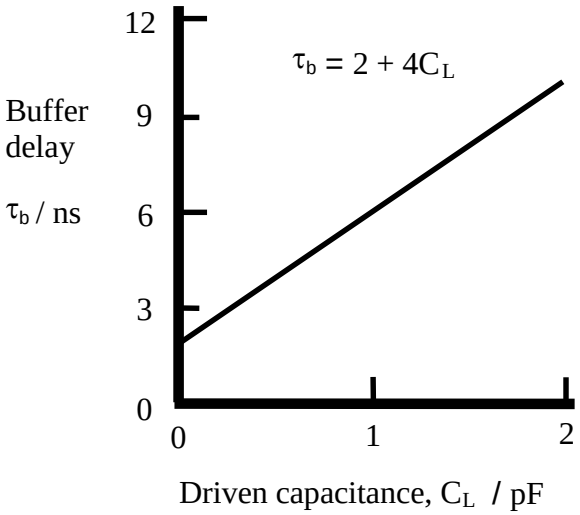

Figure 2

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Answers

1. (c) (ii) Ratio of widths p:n = 2:3; (iii) ratio of worst case rise time : fall time = 1

2.

3.

4. (b) (i) 238 mA; (ii) 594 μm

5. (b) 600 ns; (c) 209.5 ns